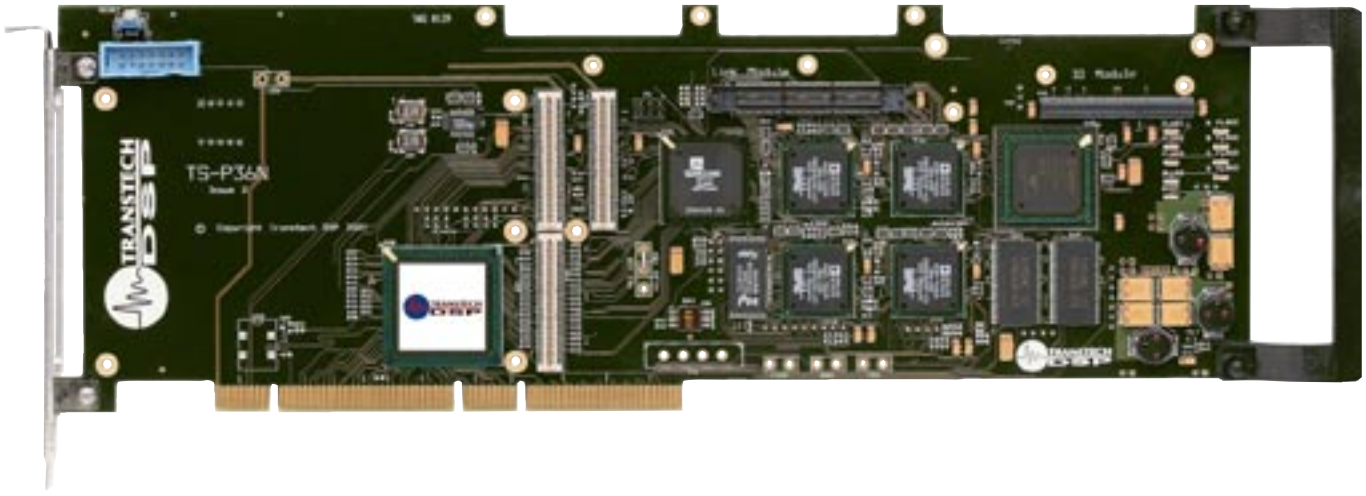
TS-P36N

Quad ADSP-TS101 DSP PCI Card with Xilinx FPGA



Features

Four 300MHz ADSP-TS101 DSPs

Clustered Architecture

32/64-bit 33/66MHz PCI Interface

PMC Site

Xilinx Virtex-II FPGA

256Mbytes Shared SDRAM

4Mbytes FLASH

VisualDSP++™ Support

Gedae & OSE Ports

The TS-P36N is a quad TIgerSHARC® DSP card providing 7.2GFLOP of performance with high-speed data I/O. Featuring a clustered architecture and fast shared memory, the TS-P36N is ideal for next generation telecommunications and real-time image processing. Incorporating a large Xilinx Virtex-II FPGA, the TS-P36N provides the developer with an additional processing resource which can also be used as a fast data port that is fully customizable for FPDP, LVDS, channel link or other digital interfaces.

TRANSTECH™ DSP

www.transtech-dsp.com

ADSP-TS101 DSP

A new generation of 32-bit floating-point processor, the TigerSHARC DSP (ADSP-TS101) is capable of up to 1800MFLOPs with four, full-duplex link ports able to operate at up to 250Mbyte/sec for inter-TigerSHARC DSP communications.

To maximize data throughput and simplify applications development, the TigerSHARC DSP natively supports multiple data types and multiple calculations per cycle. The TigerSHARC DSP can achieve six 32/40-bit floating-point, twenty-four 16-bit or forty-eight 8-bit calculations per cycle. The TigerSHARC DSP can also deal with four 32-bit instructions per cycle. This together with 6Mbits of onboard memory and parallel internal databuses mean that the TigerSHARC DSP can tackle the most demanding of applications.

Memory

In addition to the 6Mbits of SRAM on each DSP, the TS-P36N has 256Mbytes of SDRAM and 4Mbytes of FLASH. The memory is accessible by the TigerSHARC DSPs and across PCI.

For embedded applications, FLASH can be used to boot the DSP. It can be programmed across PCI by a remote task with tools are available from Transtech.

User FPGA

A Xilinx Virtex-II FPGA (XC2V1000 or XC2V3000) is available to the ADSP-TS101 DSPs for use as a co-processor to accelerate applications. The FPGA can also be used to provide a high-speed digital I/O with a choice of build options.

User FPGA

One of the key advantages of a DSP is its ability to move large amounts data quickly and efficiently. This means that a DSP board's I/O must be efficient too so as not to starve the DSP of data or cause it to wait unnecessarily. A TigerSHARC DSP based card is no exception. The TS-P36N addresses the data I/O need by providing high-speed data paths - both locally and off-board. This is achieved using both 64-bit/66MHz PCI and an FPGA resource connected directly to the TigerSHARC DSP's clusterbus. When used for I/O, the FPGA provides 64-connections to a high-density header. Since the FPGA can control the interface for one or more data streams this means that simple low cost I/O modules can be developed easily and quickly. Often these I/O modules need only contain line drivers and a suitable front panel connector.

Link Ports and Routing

Link ports, a key feature of the TigerSHARC DSP, allow high-speed point-to-point communications between other TigerSHARC DSPs. This may be on the same card or between cards. The link ports are also a convenient mechanism to allow all the DSP within the network to boot their application.

Link ports allow TigerSHARC DSP systems to adopt a wide range of topologies to best suit the application. To support this freedom, the TS-P36N provides a header to which ten link ports are routed. A link port routing module can then be fitted which is used to define the board's topology such as double pipelines, mesh, cross connected or even hypercubes. The use of routing modules means that external cables are often unnecessary. This maximizes flexibility, simplicity and improves reliability. The only link ports that the board commits is a 'boot' pipeline using a pair of links per DSP. If external links are used, headers can be positioned along the edge of the board (module dependent). Changing the configuration is as simple as changing the routing module.

Full module specifications are provided. This allows for in-house modules to be developed. Alternatively, contact Transtech for details of routing modules or ask us about providing one to meet your exact needs. Custom modules have the advantage of not only having application specific DSP routing, but also a choice of external connector.

Peak Rates at 300MHz

16-bit performance	2.4 Billion MACs/sec
32-bit fixed-point performance	600 Million MACs/sec
32-bit floating-point performance	1800MFLOPS

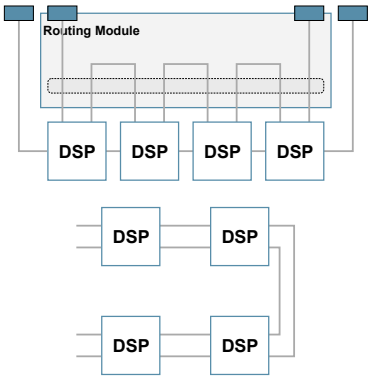
32-bit

1k cmplx FFT (radix 2)	32.78µs
50-tap FIR on 1k input	91.67µs
Single FIR MAC	1.83ns

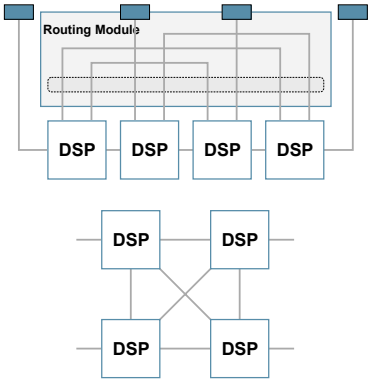
16-bit

256pt cmplx FFT (radix 2)	3.67µs
50-tap FIR on 1k input	24µs
Single FIR MAC	0.47ns
Single cmplx FIR MAC	1.9ns

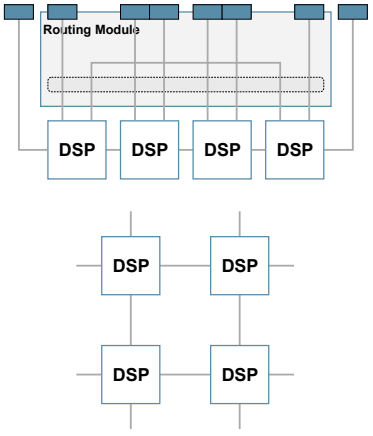
300MHz TigerSHARC DSP Benchmark Estimates



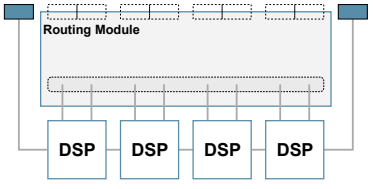
Double Pipeline
(module and effective routing)



Cross-Connected
(module and effective routing)



Mesh
(module and effective routing)



Full Breakout (module)

Link Port Routing Module Topologies

Digital I/O

The FPGA can be used to provide a high-speed digital interface via an adapter header. Modules include FPDP and LVDS. The FPDP module provides the line drivers and level-translation required and the appropriate connector through the front panel opening otherwise used by the PMC module. When using the FPDP module, the FPGA takes care of all the protocol, bus timings and data transfer.

Software Overview

Software support for the TigerSHARC DSP from Transtech deals various aspects essential for effective application development:

- *Low-level tools & utilities.*
- *Integrated Development & Debug Environments (IDDEs).*
- *Operating Systems.*

Low-Level Tools & Utilities

Bundled with the TS-P36N is a toolset of requisite utilities and library functions to compliment Analog Devices' VisualDSP++ toolset for TigerSHARC DSPs. The BSP libraries provide access to and support for Transtech DSP's board specific functions such as interrupts, DMA driven PCI interfacing as well as runtime host communications, I/O and parallel network loaders. The toolset together with VisualDSP++ provides a minimum system configuration.

Utilities

The toolset includes utility tools that simplify the development of applications running on large networks of TigerSHARC DSPs.

Network Loader

The network loader takes a DSP application (normally consisting of a network description file and a set of DSP Executables) and loads the network from the host computer's file system. Another related utility creates a single bootable output file that can be programmed into FLASH EPROM, allowing an application to be loaded onto the network of DSP processors from ROM at power up.

I/O Server

The I/O server runs on the host, loading the TigerSHARC DSP network and servicing I/O requests from the C runtime I/O library on the first TigerSHARC. The host server provides access to host I/O resources such as the console and file system, using standard ANSI C calls.

Flash Programmer

The TS-P36N allows up to 15 separate files to be loaded into FLASH which can then be retrieved, by name, by any DSP connected to the FLASH.

DSP system evaluation tool

The evaluation tool utility probes the system bus for all Transtech DSP boards. For each card, it is able to:

- *Display the complete state of the board or display a specified memory region.*
- *Perform a complete functional board test.*
- *Evaluate the system I/O performance of the board.*

System viewer (Windows only)

The system viewer provides a complete overview of the installed hardware. It is able to display all the DSP registers, all interface registers as well as Flash memory. It is suitable for post-mortem debugging and system exploration. Also included is a remote monitor for non-Windows platforms such as VxWorks.

BSP Libraries

There are a number of libraries providing support of the board hardware with both high-level routines for quick coding and also lower-level routines that allow communications to be optimized.

C Runtime I/O Library

A full ANSI standard library is provided for screen and file I/O from C code running on the first DSP in the network. This allows a very simple way for new users to get code up and running on the boards and provides a useful base for simple system development.

Software Summary

- **Transtech Tools**
  Hardware specific libraries
  Target/Host communications
  Loader and network utilities
- **VisualDSP++™**
  GUI-based IDE
  EPC Toolschain
  Multi-processor debugging
  Project Management
- **Gedae™**
  Self-contained high level graphical development
  Multi-processor/multi-processing
- **VSPWorks/Virtuoso™**
  Real-Time Operating System
  Multi-processor/multi-processing
  Virtual single processor model
- **Third Party Libraries**
  Hand optimized DSP
  I/O modules drivers

Host Application Libraries

Host based C++ libraries allow the writing of applications that boot a network of TigerSHARC DSPs. The libraries also support hardware access so that the host can read/write DSP internal memory, Flash and any register.

Board Support Library

To fully support the TS-P36N hardware, Transtech provides an I/O library. This includes routines to allow the TigerSHARC DSP access to other PCI cards in the system (via single cycle peek/poke cycles or high performance DMA) as well as supporting FPDP and other peripheral hardware.

Debuggers

A JTAG header is provided on the TS-P36N to ease debugging. This allows an Analog Devices emulator to be used with the VisualDSP++ debug tools and allows single or multi-processor debugging. Emulator hardware is also available from Transtech DSP.

VisualDSP++

The latest tools from Analog Devices support software development for the latest TigerSHARC DSPs. The VisualDSP++ tool suite provides an integrated environment for developing DSP applications and also a flexible management system for DSP projects. It includes:

- *Integrated Development and Debugging Environment (IDE).*
- *C/C++ optimizing compiler with run-time library.*
- *Assembler and linker*
- *Simulator software with sample programs.*
- *Combined debugging and project management environments provide a single user interface for both development and debugging.*
- *Linear profiling: a debug technique that samples the target's PC register at every instruction cycle to accurately measures where instructions were executed.*

IDE

The integrated development, project management and debugging environment provides complete graphical control of the edit, build, and debug process.

Development Tools

VisualDSP++ includes a C/C++ compiler, assembler, linker, preprocessor, archiver and run-time library. VisualDSP++ supports ELF/DWARF-2 executable files. The debugger allows the developer to:

- *View and debug mixed C/C++ and assembly code.*
- *Run TCL command-line scripts using Tool Command Language (TCL) version 8.3 to customize key debugging features.*
- *Use memory expressions that reference memory.*
- *Use breakpoints to view registers and memory.*
- *Statistically profile the target processor's PC while emulating.*
- *Linearly profile the target processor's PC while simulating.*
- *Graphically plot values from DSP memory.*

Run Time Libraries

Supplied with VisualDSP++ are C and C++ run-time libraries that are collections of functions, macros, and class templates that can be called from source programs. Many functions are implemented in the DSP's assembly language. Included in the package is a broad collection of C functions encompassing those required by the ANSI standard and additional Analog Devices-supplied functions of value for DSP programming.

In addition to the Standard C Library, the latest releases now include the abridged library, a conforming subset of the Standard C++ Library.

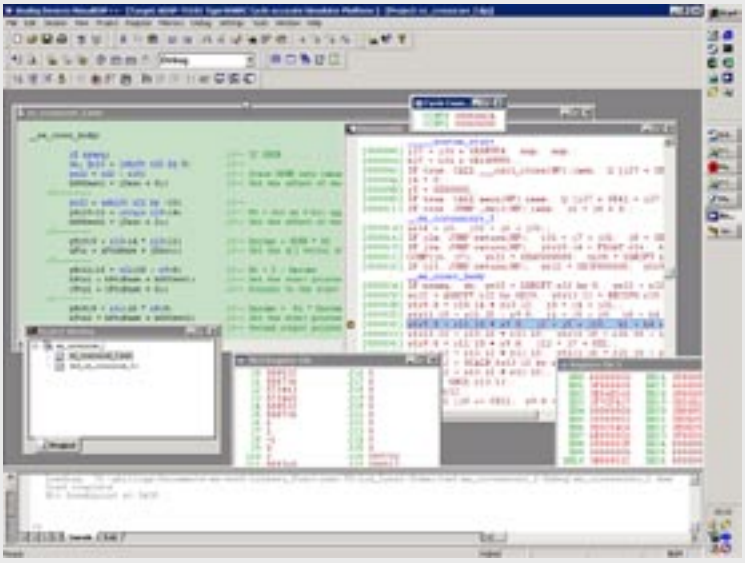
Host Operating System Support

The host services provided by the libraries described above usually require the support of an operating system dependent device driver. The following operating systems are currently supported by a driver for the TS-P36N:

Windows NT4/2000

Optimized DSP Library for TigerSHARC DSP

TS-Lib is an extensive, hand-optimized assembly language library for the TigerSHARC DSP. Designed to complement Analog Devices' run-time library (included within the VisualDSP++ tool-chain) it contains over 400 functions for signal and image processing applications.



Power Routines
Scalar, Vector, Complex Scalar Power, Complex Vector

Trigonometric Routines
Scalar & Vector Trigonometric, Scalar & Vector Hyperbolic

Vector Mathematic Routines
2-input term Vector & complex Vector, 3-input term Vector & Complex Vector, 4-input term Vector

Matrix Mathematic Routines
Matrix Vector & Scalar, Complex Matrix-Vector & Scalar

Simple Operations
Scalar, Vector, Complex Scalar, Complex Vector

Logic-Test-Sort Operations
Vector Test, Threshold, Logic, Shift, Sorting, Matrix Check

Statistic Operations
Vector Sum/Average, Vector Max/Min, Matrix Max/Min, Probability, Vector Gather/Scatter, Histogram, Integration, Interpolation

Filter Routines
Convolution, Correlation, Filtering, Windowing

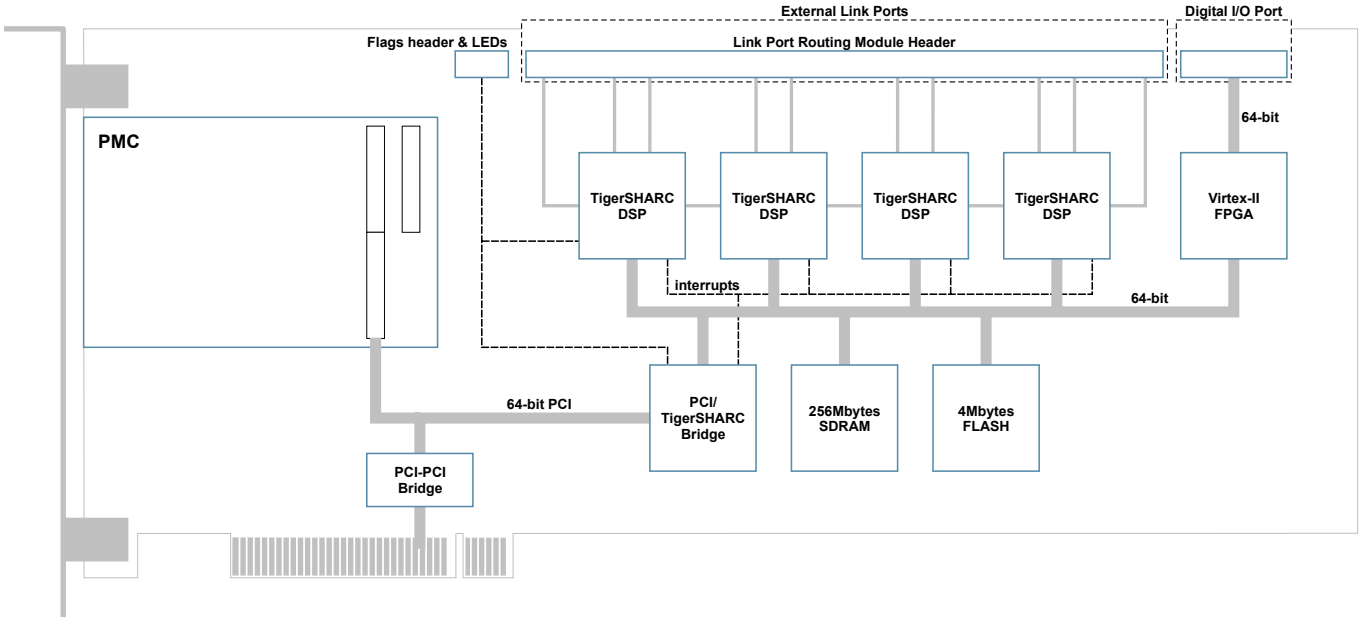
Transform Routines
Conversion, Complex FFTs, Real FFTs, FFT Operator, DCT Routines, Compander, Coordinate Transform, Accumulating Spectrum

Matrix/Vector Creation & Moving Routines
Create Matrix / Vector, Complex Vector Creation, Distribution and Pseudo-Random Number Generation, Memory Move, Matrix/Vector

Other Routines
Doppler, Cholesky, Signal-Noise , Sub-matrix

TS-Lib is made available in association with EZ-DSP Ltd

Block Diagram



Technical Specification

DSP

Type	ADSP-TS101 (TIgerSHARC® DSP)
Number	1 or 4
Clock Speed	300MHz
Link Port Routing	10 - routed to header for link port routing module
Link Port Bandwidth	250Mbytes/sec per port

Memory

ADSP-TS101S (on-chip)	6Mbits
SDRAM	256Mbytes
FLASH	4Mbytes Used to boot DSPs and store FPGA configuration. Programmable via PCI interface

PCI

Local PCI Device	TS-PCI
Compliance	32/64-bit PCI 2.2 33/66MHz, master/slave/DMA
Enhancements	Endian swapping, DMA, interrupt support
Bandwidth	up to 528Mbytes/sec

PMC Site

Number	1
Compliance	64-bit/66MHz, 3.3/5V signalling

FPGA/Digital I/O Header

Device	Xilinx Virtex-II XC2V1000 or 3000
Package	FG456 or FG676
I/O Connector	Samtec CLE-150-01-G-DVA
Connectivity	64 user I/O signals
I/O Modules	FPDP, LVDS, channel link, custom

Debugging

JTAG header	14-pin DIL header adaptor

Misc

External TigerSHARC DSP flags with LEDs

Power

5V/3.3V	14W

Software Support

Development tools	VisualDSP++™, Transtech utilities
Native Operating Systems	Gedae, VSPworks™, OSE
Run-time OS Support	Windows NT/2000
Other	Signal and Image Processing Library (TS-Lib)

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