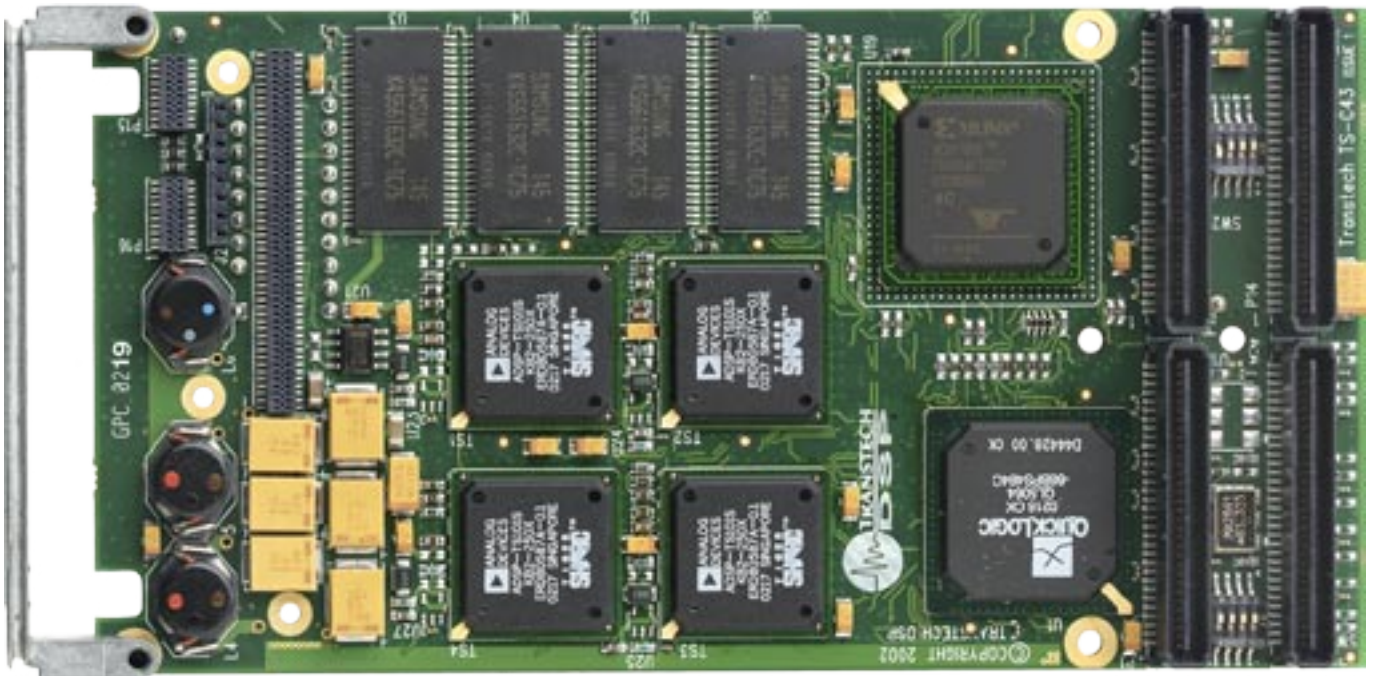


TS-C43

Quad ADSP-TS101S DSP 64-bit PMC Card



Features

4x 300MHz ADSP-TS101 DSPs

Clustered Architecture

32/64-bit (33/66MHz) PCI Interface

Local Xilinx Virtex-II™ FPGA

FPDP, SERDES and Channel Link
Digital I/O options

256Mbytes Shared SDRAM

4Mbytes FLASH

VisualDSP++™ Support

The TS-C43 is a quad TigerSHARC® DSP PMC module providing over 7GFLOPs of performance with high-speed data I/O. Featuring a clustered architecture and fast shared memory, the TS-C43 is ideal for next generation telecommunications and real-time image processing. Incorporating a Xilinx Virtex-II FPGA, the TS-C43 provides the developer with an additional processing resource which can also be used as a fast data port that is fully customizable for FPDP, LVDS, channel link or other digital interfaces.



www.transtech-dsp.com

ADSP-TS101 DSP

The TigerSHARC DSP (ADSP-TS101) is capable of 1.8GFLOPs with four, full-duplex 250Mbyte/sec link ports (local) for inter-TigerSHARC DSP communications.

To maximize data throughput and simplify applications development, the TigerSHARC DSP natively supports multiple data types and multiple calculations per cycle. The TigerSHARC DSP can achieve six 32/40-bit floating-point, twenty-four 16-bit or forty-eight 8-bit calculations per cycle. The TigerSHARC DSP can also deal with four 32-bit instructions per cycle. This together with 6Mbits of onboard memory and parallel internal databuses mean that the TigerSHARC DSP can tackle even the most demanding of applications.

Memory

In addition to the 6Mbits of SRAM on each DSP, the TS-C43 has 256Mbytes of SDRAM and 4Mbytes of FLASH. This memory is accessible to both the TigerSHARC DSPs and the PCI interface.

For embedded applications, the FLASH can be used to boot the DSP. It can also be programmed across PCI by a remote task. These tools are available from Transtech.

User FPGA & Digital I/O

A Xilinx Virtex-II FPGA is available to the ADSP-TS101 DSPs for use as a co-processor to accelerate applications. By default the user FPGA is an XC2V1000 device - contact Transtech DSP for larger devices.

As an alternative to a co-processor, the FPGA can be used to provide a high-speed digital interface via an adapter header. Ready developed modules that Transtech supply include FPDP and channel link. The FPDP module provides the line drivers and level-translation required and the appropriate connector through the front panel opening otherwise used by the PMC module. When using the FPDP module, the FPGA takes care of all the protocol, bus timings and data transfer. Using a similar strategy, a range of low cost custom modules can also be developed.

Link Ports

Link ports, a key feature of the TigerSHARC DSP, allow high-speed point-to-point communications between other TigerSHARC DSPs. This may be on the same card or between cards. The link ports are also a convenient mechanism to allow all the DSP within the network to boot their application.

The TS-C43 provides four off-board link ports available through either the front panel or via the PMC user I/O connector. The link ports are routed via the Xilinx FPGA device. In addition, every DSP has a direct link port connection with every other DSP.

Software Overview

Software support for the TigerSHARC DSP from Transtech deals various aspects essential for effective application development:

- Low-level tools & utilities.
- Integrated Development & Debug Environments (IDEs).
- Operating Systems.

Peak Rates at 300MHz

16-bit performance	2.4 Billion MACs/sec
32-bit fixed-point performance	600 Million MACs/sec
32-bit floating-point performance	1800MFLOPS

32-bit

1k cmplx FFT (radix 2)	32.78µs
50-tap FIR on 1k input	91.67µs
Single FIR MAC	1.83ns

16-bit

256pt cmplx FFT (radix 2)	3.67µs
50-tap FIR on 1k input	24µs
Single FIR MAC	0.47ns
Single cmplx FIR MAC	1.9ns

300MHz TigerSHARC DSP
Benchmark Estimates



Dual site 32/64-bit PMC carrier

Low-Level Tools & Utilities

Bundled with the TS-C43 is a toolset of requisite utilities and library functions to compliment Analog Devices' VisualDSP++ toolset for TigerSHARC DSPs. The BSP libraries provide access to and support for Transtech DSP's board specific functions such as interrupts, DMA driven PCI interfacing as well as runtime host communications, I/O and parallel network loaders. The toolset together with Analog Devices' VisualDSP++ provides a minimum system configuration.

Utilities

The toolset includes utility tools that simplify the development of applications running on large networks of TigerSHARC DSPs.

Network Loader

The network loader takes a DSP application (normally consisting of a network description file and a set of DSP Executables) and loads the network from the host computer's file system. Another related utility creates a single bootable output file that can be programmed into FLASH EPROM, allowing an application to be loaded onto the network of DSP processors from ROM at power up.

I/O Server

The I/O server runs on the host loading the DSP network and servicing I/O requests from the C runtime library on the first DSP. The host server provides access to host I/O resources such as the console and file system, using standard ANSI C calls.

Flash Programmer

The TS-C43 allows up to 15 separate files to be loaded into FLASH which can then be retrieved, by name, by any TigerSHARC DSP connected to the FLASH.

DSP system evaluation tool

The evaluation tool utility probes the system bus for all Transtech DSP boards. For each card found, it is able to:

- *Display the complete state of the board or display a specified memory region.*
- *Perform a complete functional test of the board.*
- *Evaluate the system I/O performance of the board.*

System viewer (Windows only)

The system viewer provides a complete overview of the installed TigerSHARC DSP hardware. It is able to display all TigerSHARC DSP registers, all interface registers as well as Flash memory. It is suitable for post-mortem debugging and system exploration. Also included is a remote monitor for non-Windows platforms such as VxWorks.

BSP Libraries

There are a number of libraries providing support of the board hardware with both high-level routines for quick coding and also lower-level routines that allow communications to be optimized.

C Runtime I/O Library

A full ANSI standard library is provided for screen and file I/O from C code running on the first TigerSHARC DSP in the network. This allows a very simple way for new users to get code up and running on TigerSHARC DSP boards and provides a useful base for simple system development.

Host Application Libraries

Host based C++ libraries allow the writing of applications that boot a network of TigerSHARC DSPs. The libraries also support general hardware access so that the host can read/write SHARC DSP internal memory, Flash and any register.

Software Summary

■ **Transtech Tools**

Hardware specific libraries
Target/Host communications
Loader and network utilities

■ **VisualDSP++™**

GUI-based IDE
EPC Toolschain
Multi-processor debugging
Project Management

■ **Gedae™**

Self-contained high level
graphical development
Multi-processor/multi-processing

■ **VSPWorks/Virtuoso™**

Real-Time Operating System
Multi-processor/multi-processing
Virtual single processor model

■ **Third Party Libraries**

Hand optimized DSP
I/O modules drivers

Board Support Library

To fully support the TS-C43 hardware, Transtech provides an I/O library. This includes routines to allow the TigerSHARC DSP access to other VME, cPCI and PCI cards (fitted to a TPMB2 host) in the system (via single cycle peek/poke cycles or high performance DMA) as well as supporting FPDP and other peripheral hardware.

Debuggers

A JTAG header is provided on the TS-C43 to ease debugging. This allows an Analog Devices emulator to be used with the VisualDSP++ debug tools and allows single or multi-processor debugging. Emulator hardware is also available from Transtech DSP.

VisualDSP++

The latest tools from Analog Devices support software development for the latest TigerSHARC DSPs. The VisualDSP++ tool suite provides an integrated environment for developing DSP applications and also a flexible management system for DSP projects. It includes:

- *Integrated Development and Debugging Environment (IDE).*
- *C/C++ optimizing compiler with run-time library.*
- *Assembler and linker*
- *Simulator software with sample programs.*
- *Combined debugging and project management environments provide a single user interface for both development and debugging.*
- *Linear profiling: a debug technique that samples the target's PC register at every instruction cycle to accurately measure where instructions were executed.*

IDE

The integrated development, project management and debugging environment provides complete graphical control of the edit, build, and debug process.

Development Tools

VisualDSP++ includes a C/C++ compiler, assembler, linker, preprocessor, archiver and run-time library. VisualDSP++ supports ELF/DWARF-2 (Executable Linkable Format) executable files. The debugger allows the developer to:

- *View and debug mixed C/C++ and assembly code.*
- *Run TCL command-line scripts using Tool Command Language (TCL) version 8.3 to customize key debugging features.*
- *Use memory expressions that reference memory.*
- *Use breakpoints to view registers and memory.*
- *Statistically profile the target processor's PC while emulating.*
- *Linearly profile the target processor's PC while simulating.*
- *Graphically plot values from DSP memory.*

Run Time Libraries

Supplied with VisualDSP++ are C and C++ run-time libraries that are collections of functions, macros, and class templates that can be called from source programs. Many functions are implemented in the DSP's assembly language. Included in the package is a broad collection of C functions encompassing those required by the ANSI standard and additional Analog Devices-supplied functions of value for DSP programming.

In addition to the Standard C Library, the latest releases now include the abridged library, a conforming subset of the Standard C++ Library.

Host Operating System Support

The host services provided by the libraries described above usually require the support of an operating system dependent device driver. Run-time drivers for the TS-C43 support include the following operating systems:

- Windows NT4/2000
- VxWorks/PowerPC MVME5100

Optimized DSP Library for TigerSHARC DSP

TS-Lib is an extensive, hand-optimized assembly language library for the TigerSHARC DSP. Designed to complement Analog Devices' run-time library (included within the VisualDSP++ tool-chain) it contains over 400 functions for signal and image processing applications.

Power Routines

Scalar, Vector, Complex Scalar Power, Complex Vector

Trigonometric Routines

Scalar & Vector Trigonometric, Scalar & Vector Hyperbolic

Vector Mathematic Routines

2-input term Vector & complex Vector, 3-input term Vector & Complex Vector, 4-input term Vector

Matrix Mathematic Routines

Matrix Vector & Scalar, Complex Matrix-Vector & Scalar

Simple Operations

Scalar, Vector, Complex Scalar, Complex Vector

Logic-Test-Sort Operations

Vector Test, Threshold, Logic, Shift, Sorting, Matrix Check

Statistic Operations

Vector Sum/Average, Vector Max/Min, Matrix Max/Min, Probability, Vector Gather/Scatter, Histogram, Integration, Interpolation

Filter Routines

Convolution, Correlation, Filtering, Windowing

Transform Routines

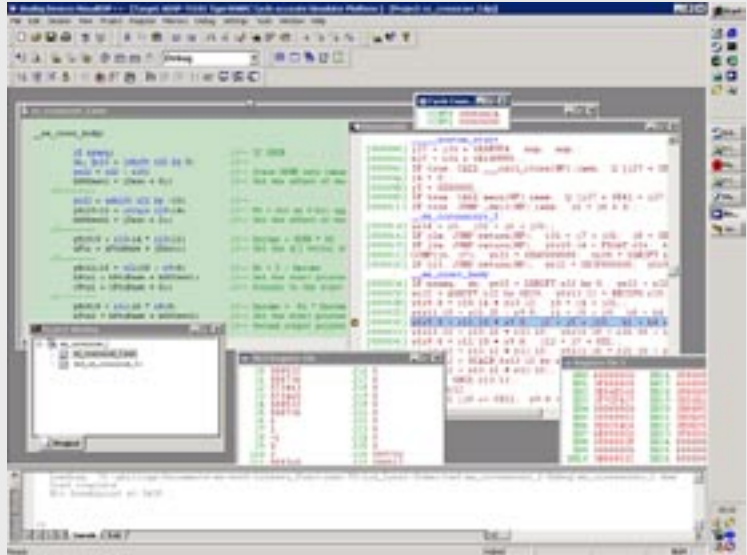
Conversion, Complex FFTs, Real FFTs, FFT Operator, DCT Routines, Compander, Coordinate Transform, Accumulating Spectrum

Matrix/Vector Creation & Moving Routines

Create Matrix / Vector, Complex Vector Creation, Distribution and Pseudo-Random Number Generation, Memory Move, Matrix/Vector

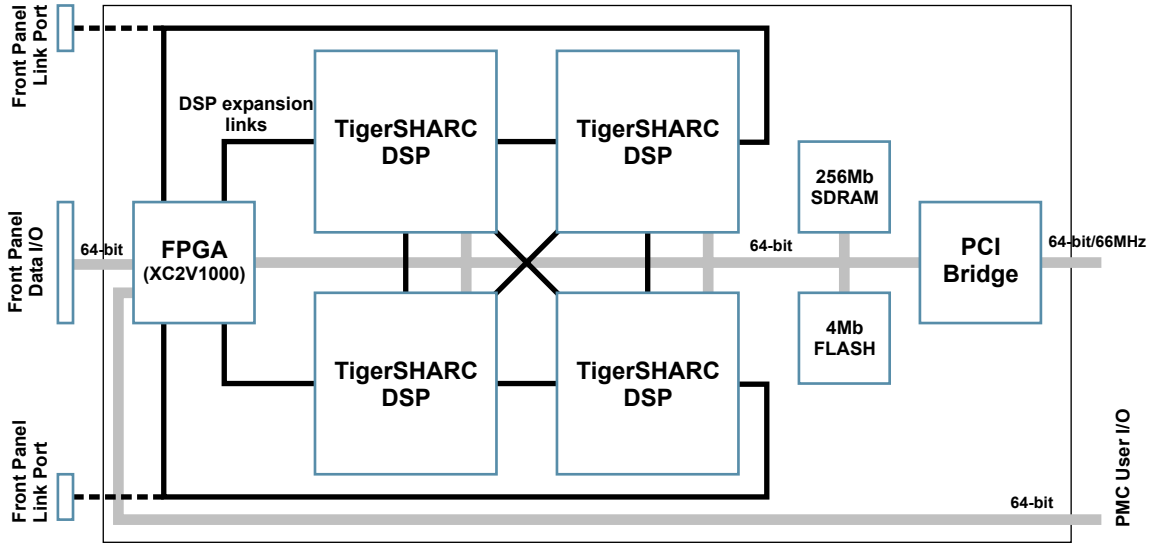
Other Routines

Doppler, Cholesky, Signal-Noise, Sub-matrix



TS-Lib is made available in association with EZ-DSP Ltd

Block Diagram



Specification

DSP

Type	ADSP-TS101 (TigerSHARC® DSP)
Number	4
Clock Speed	300MHz
Link Port Routing	4 - through front panel or PMC P14 connector (note: signal are routed via FPGA device)
Link Port Bandwidth	250Mbytes/sec per port

Memory

ADSP-TS101S (on-chip)	6Mbits
SDRAM	256Mbytes
FLASH	4Mbytes Used to boot DSPs and store FPGA configuration. Programmable via PCI interface

PCI

Local PCI Device	TS-PCI
Compliance	32/64-bit PCI 2.2 33/66MHz, master/slave/DMA
Enhancements	Endian swapping, DMA, interrupt support
Bandwidth	up to 528Mbytes/sec

FPGA/Digital I/O Header

Device	Xilinx XC2V1000 Virtex-II FPGA
I/O Connector	Samtec CLE-150-01-G-DVA
Connectivity	64 I/O signals (front panel via an I/O adaptor module) plus 64 to PMC user IO connector
I/O Modules	FPDP, SERDES, channel link, custom

Debugging

JTAG header	14-pin DIL header adaptor
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Misc

External TigerSHARC DSP flags with LEDs	
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Power

Typical	10W
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Software Support

Development tools	VisualDSP++, Transtech utilities
Native Operating Systems	Virtuoso, OSE, GEDAE
Run-time OS Support	Windows NT/2000, VxWorks
Other	TS-Lib (over 400 optimized signal & image processing functions) Third party libraries including 3G telecommunications

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