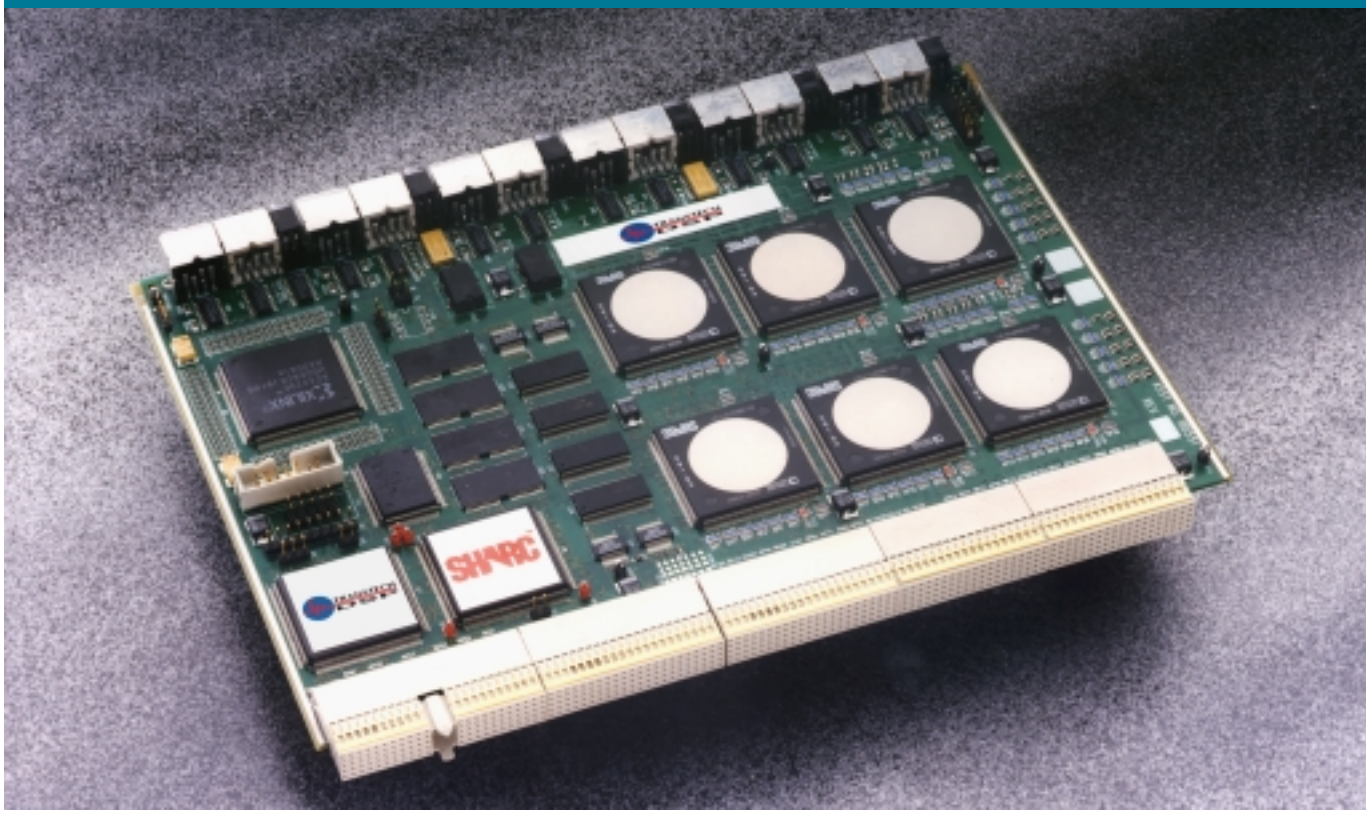
ASP-S60

Hex SHARC Processor Engine



Aimed at high performance, floating-point DSP applications, the ASP-S60 merges the power of six SHARC DSPs with the speed of CompactPCI and front end processing of a Xilinx XC4028EX FPGA. The result is a highly flexible processing engine ideally suited to professional audio, sonar and telecommunications applications.

The architecture and connectivity of the ASP-S60 is simple: twelve differential SPORTs driven by a Xilinx FPGA, which is connected to a cluster of SHARCs. In addition to the CompactPCI connector, the ASP-S60 supports additional backplane connectors to carry all thirty-six SHARC link ports. This allows a wide range of architectures to be supported when used with an appropriate backplane design - *flexibility and performance without compromise.*

- **Six 40MHz SHARC DSPs**
- **Xilnix 4028EX FPGA**
- **SHARC Clustered Architecture**
- **32-bit PCI Interface**
- **12x 40Mbit/sec SPORTs**
- **EZ-ICE Emulator Compatible**
- **36x 40Mbyte/sec Link Ports**
- **6U CompactPCI Format**
- **8Mbytes Shared DRAM**
- **Ideal for Sonar and Pro Audio**

Overview

ADSP-2106x DSP

At the heart of the ASP-S60 lies six 40MHz ADSP-2106x DSPs arranged in a cluster architecture with 8Mbytes of shared DRAM. SHARC features include:

- 32-bit floating-point core
- 2 or 4Mbits of dual-ported SRAM
- 6x 40Mbyte/sec link ports
- 10-channel DMA controller
- 2x 40Mbit/sec serial ports
- JTAG debug port

On-chip SRAM

The ASP-S60 offers a choice of ADSP-21062 or ADSP-21060 SHARC DSP offering 2 or 4Mbits of SRAM respectively. For many applications, the 2 or 4Mbits of on-chip SRAM is enough capacity to fit the entire program and storage requirements - in such circumstances, this allows maximum performance at minimum cost.

DRAM

Fitted as standard is 8Mbytes of 32-bit wide DRAM which is accessible by any of the SHARC DSPs and the 32-bit PCI bus (CompactPCI).

Link Port Connectors

Each ADSP-2106x DSP has six 40Mbyte/sec communication channels which are able to operate concurrently and designed to inter-connect SHARCs. These allow SHARC based systems to be scaled and optimized for a wide range of applications.

In the case of the ASP-S60, all thirty-six link ports are routed to the user I/O pins provided by the backplane connectors. This allows maximum flexibility in routing strategies between SHARCs on the same ASP-S60 or on other ASP-S60s.

Serial Ports (SPORTs)

The ASP-60 supports six external SPORT connections available through twelve front panel connectors, six for input and six for output. Each SPORT is routed via a Xilinx FPGA which has access to both SPORT channels of all six SHARC devices.

SPORTS provide 40Mbit/sec, full duplex synchronous communications, word lengths of up to 32-bits and programmable A-law and µ-law companding.

Each external SPORT connection is differentially driven. By using differential SPORTs, the ASP-S60 improves both noise immunity and increases the distance of connection to peripherals.

Xilinx 4028EX FPGA

The ASP-S60's on board FPGA allows front-end pre-processing and routing of data on all SPORT channels. This allows a high degree of control in being able to dynamically move data between SPORTs or change application configurations. The FPGA also allows for the off-loading of unsophisticated, but compute intensive tasks from the SHARC DSPs.

The Xilinx 4028EX FPGA is also capable of interrupting each SHARC.

Uses for FPGA include flittering, FFTs, data calibration, lookup tables.

Cluster Bus

The ASP-S60 implements all the features of the SHARC clustering bus, including:

- every SHARC can access any other SHARC's onboard memory
- SHARC broadcasting enabling simultaneous writing to all SHARC during a single cycle
- full access to shared DRAM

CompactPCI Interface

The ASP-S60 supports a 32-bit master/slave PCI interface. The CompactPCI interface has access to onboard resources including SHARC memory and a port to the Xilinx FPGA.

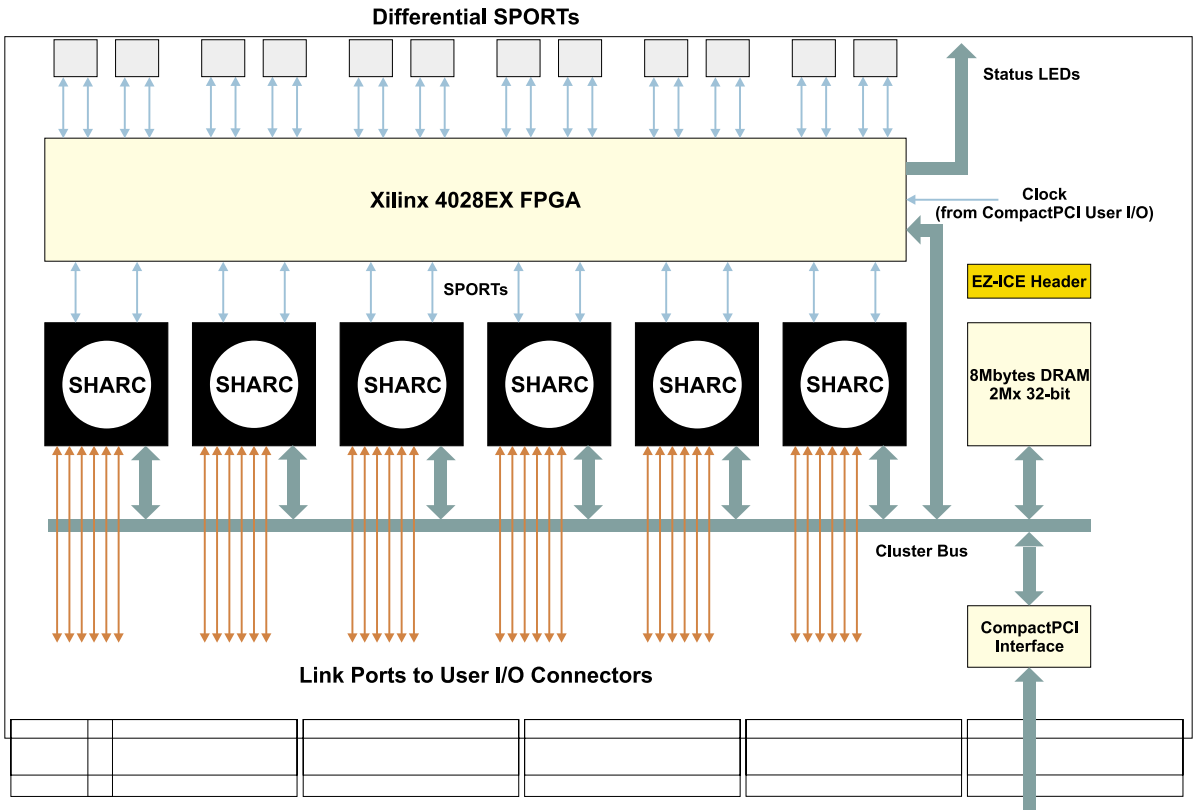
Custom Backplanes

Using the ASP-S60's SHARC DSP link ports requires a dedicated custom backplane to provide routing. Since each system may have a different confiuration, it has been left to the customer to provide this.

If not used with a custom backplane, the ASP-S60 can only be used in a compactPCI backplane with only J1 and J2 headers fitted. This is because the ASP-S60's J3-5 connectors do not comply with the usual compactPCI definitions. Used in this way, the ASP-S60's SHARC DSP link port connectors are not available.

EZ-ICE Header

ASP-S60 incorporates an EZ-ICE header to provide in-circuit emulation via JTAG. To use this facility, an EZ-ICE probe and PC-ISA add-in card (available separately) is required. This combination provides the basis for a complete development and debug environment. Using EZ-ICE allows C-source level debugging within a GUI interface



ASP-S60 Block Diagram

and complete control over loading, execution and inspection of program variables.

An alternative to the Analog Devices' EZ-ICE probe/ISA card combination is White Mountain DSP's Mountain-ICE - available directly from Transtech. White Mountain DSP also produce an Sbus solution.

Software Support

Transtech SHARC products are supported by Transtech's ASP-Toolset. Xilinx FPGA code development requires Xilinx development tools.

ASP-Toolset

The Analog Device toolset for developing SHARC applications provides the foundation to the ASP-Toolset. This includes an assembler, C-compiler, linker, librarian, simulator and debugger for PC or Sun hosts.

By extending these tools, the ASP-Toolset adds essential network utilities and host I/O server support allowing processors access to off-board resources. This combination allows sophisticated SHARC code development at low cost.

Technical Specification

Overview

Architecture	Hex SHARC cluster
Format	6U CompactPCI
Bus Bandwidth	240Mbytes/sec
DSP Processor	ADSP-21060 or ADSP-21062
Clock Speed	40MHz
DMA	10 channel (on-chip), 240Mbytes/sec

Memory

On-chip Memory (per processor)	4Mbits (ADSP-21060), 2Mbits (ADSP-21062)
DRAM	2Mx32-bit (8Mbytes)

Link Ports

External	36: 6 per SHARC
Bandwidth	40Mbytes/sec
External Connector	Mapped J3-J5 user I/O connectors (Note: Requires custom backplane)

SPORTs

Total	12: 2 per SHARC, routed via FPGA
TDM mode	yes - via Xilinx 4028EX FPGA
Bandwidth	40Mbits/sec
Electrical Format	Differential TTL
Connector	Input: AMP 749179-1 Output: AMP 786767-1

CompactPCI Interface

Compliance	Rev 2.0 (master/slave)
Data Width/Clock	32-bit PCI/33MHz

EZ-ICE/Mountain-ICE™ Debug Port

Connector	14-way 0.1" key IDC header

Power Requirement

5V	TBA

Software

ASP-Toolset

Contact Transtech for details

Ordering Information

ASP-S60-6-x **where x : processor type - 2 = ADSP-21062, 4 = ADSP-21060**

For example: *ASP-S60-6-4*
Hex ADSP-21060 CompactPCI board with 8Mbytes DRAM

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