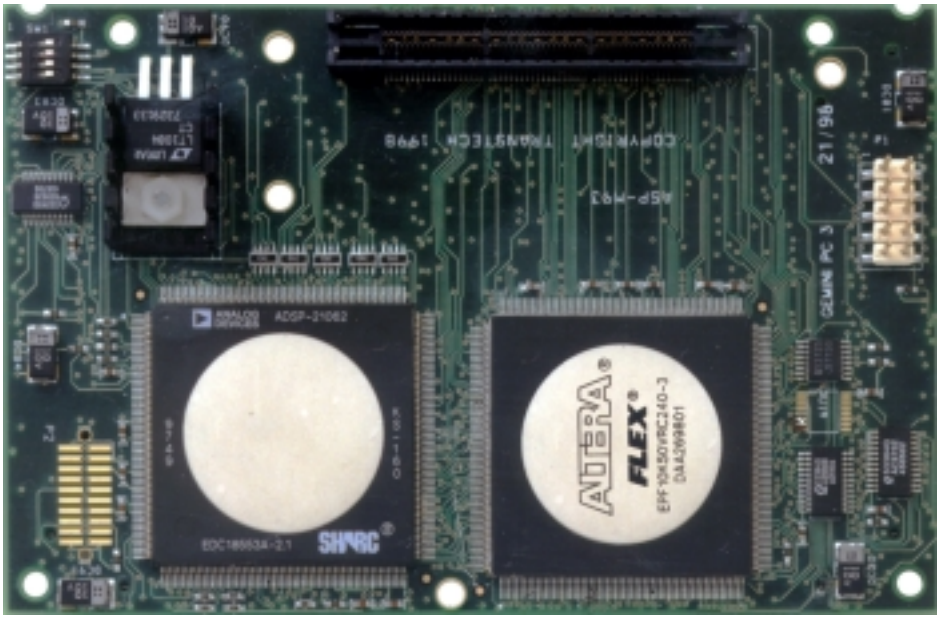
ASP-M93

FPGA Based Digital I/O SHARCPAC Module



The ASP-M93 provides high speed digital I/O to SHARC DSP based boards at up to 160Mbytes/sec via an FPGA and ADSP-2106x processor. The ASP-M93 is aimed at applications for including radar, sonar and real-time imaging processing.

Freely configurable for either input or output, the ASP-M93 provides up to 90 TTL I/O channels through a 114-pin Mictor™ connector. The I/O channels can be configured as individual bits or as groups. The ASP-M93 not only allows for fully programmable digital I/O, but can also accommodate high speed front end processing such as FFTs, digital filtering and data reduction. In combination with an Altera FLEX or Xilinx Virtex FPGA, a local SHARC provides a 120MFLOP DSP and comms ports to SHARC arrays and other processors.

- Virtex XCV50 FPGA Option
- ADSP-2106x SHARC DSP
- FLEX 10K FPGA Option
- FPDP I/O Adaptor
- 90-pin Digital I/O
- Programmable FPGA Clock
- 64/128Mbytes of fast SDRAM
- Input/Output FIFOs
- 512Kbytes FLASH
- SHARCPAC Format

The FPGA Advantage

FPGAs feature an array of gates, logic and memory cells which can be freely connected together to form more complex application specific functions - in effect FPGAs combine much of the benefits of software flexibility with the speed of hardware. In this way FPGAs can offer a range of advantages over conventional methods - in particular, speed and flexible hardware.

Key tasks that an FPGA could be used for on an ASP-M93 include:

- **High speed digital interface**
  radar, digital camera, FPDP, etc.
- **Digital Signal Processing**
  FFTs, filters, decoders, etc.
- **Imaging**
  convolutions, correlation, edge detection, translation, etc.

Coupling the FPGA with a SHARC DSP allows high speed digital I/O to be acquired (with optional front-end pre-processing) and pipelined into high performance DSP arrays. The digital I/O can be used for single or parallel data streams and have the option of being customised.

Choice of FPGA

The ASP-M93 can be fitted with either Altera 10K100A-1/10K30A-3 or Xilinx Virtex XCV50 FPGAs for a choice in complexity, speed and cost. To support high speed data throughput using the Altera FPGA option, bi-directional FIFOs are inlcuded. The Virtex variant support on-chip FIFOs.

FPGA Software Support

Transtech SHARC products are supported by Transtech's ASP-Toolset and provides the basis for ASP-M93 code development.

Altera FLEX 10K

To produce code for an Altera FPGA, the MAX+PLUS II development tools are available directly from Altera. Full details are available from Altera (www.altera.com).

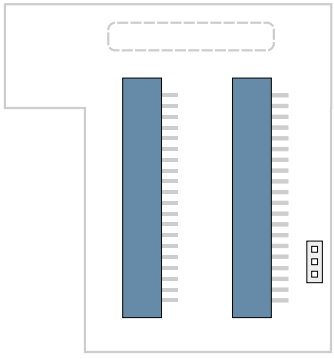
Xilinx Virtex™

Suitable synthesis tools for the Virtex FPGAs are available from Synplicity with their Synplify™ package. Full details of these tools are available from http://www.synplicity.com

I/O Adaptor Modules

The ASP-M93 uses a 114-pin Mictor connector to attach user I/O modules - 90 of these pins are available for I/O. Since the interface timings can be handled by the FPGA, adapter modules can be very simple needing only to provide the appropriate buffering, level conversion and correct connector.

A simple I/O module is available from Transtech DSP which provides



ASP-M93 Breakout Module

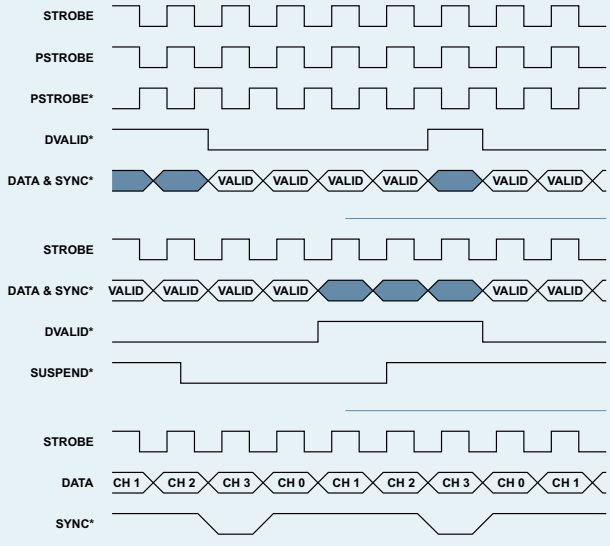
access to 50 I/O signals through two 40-way IDC headers.

FPDP Background

Developed by ICS in 1994, FPDP is a 32-bit parallel synchronous interface for pipelining data at up to 160Mbytes/sec+. FPDP was defined with simplicity and cost in mind. The use of an 80-way ribbon cable interconnect and single direction data transfers reflects this. With this level of performance and ease of use, FPDP makes a compelling alternative to expensive and difficult to use bussed architectures.

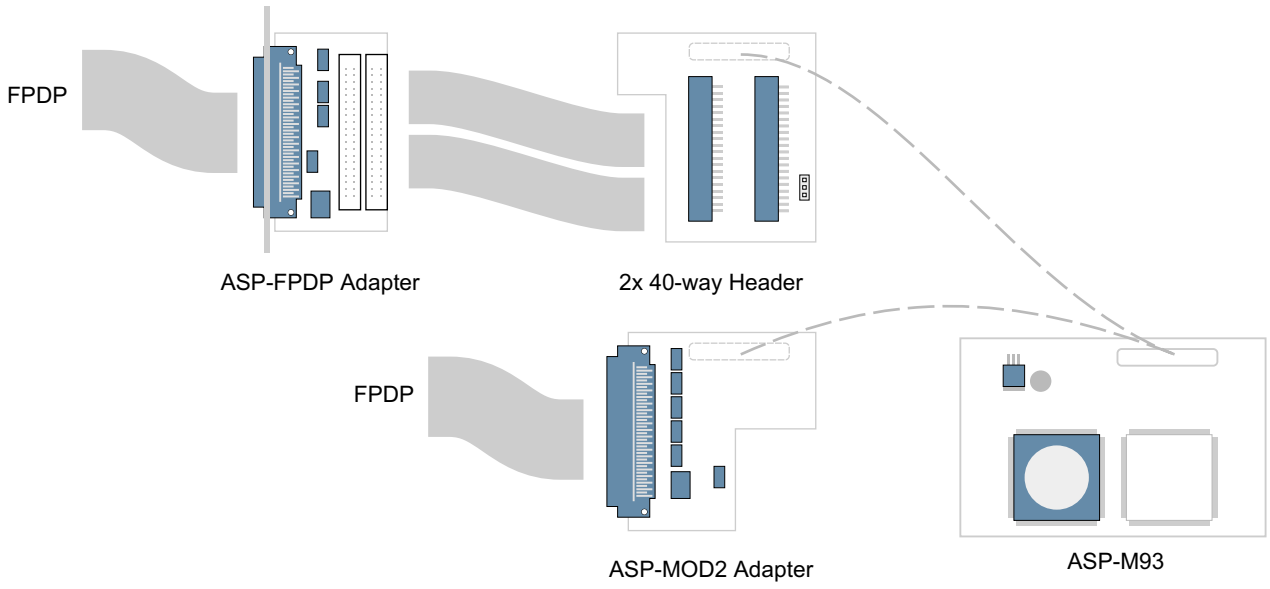
FPDP is an open standard adopted by multiple vendors including Transtech DSP. FPDP lists three types of interface: FPDP/TM (Transmit Master), FPDP/RM (Receive Master) and FPDP/R (Receive). Boards able to switch between these modes are also permitted.

Other features of FPDP include the ability to support multiple data channels, multi-drop capability for several receivers to acquire system wide data and cable lengths of up to 2m (TTL strobe) or 5m (PECL strobe).



FPDP Timings

The VITA Standards Organization ANSI/VITA 17 standard, which specifies FPDP, is available from:
VMEbus International Trade Association, 7825 E. Gelding Drive, Suite 104, Scottsdale, AZ 85260, USA



FPDP I/O Options

FPDP I/O

Front Panel Data Port (FPDP) has become a standard interface for high speed acquisition systems to transfer data. FPDP define a 32-bit data bus supporting bandwidths of up to 160Mbytes/sec across a ribbon cable. Not needing a backplane, FPDP is a low cost flexible solution that can be used VME, PCI or any number of system formats.

To support FPDP, the ASP-M93 has a choice of two adaptor modules: internal (ASP-MOD2) for FPDP connections which do not require to be passed through a bulkhead panel and external (ASP-FPDP) which fits onto the default header module and can be mounted through a system panel. The internal module is ideal for connection within a PCI board set and the external option is suitable for VME systems.

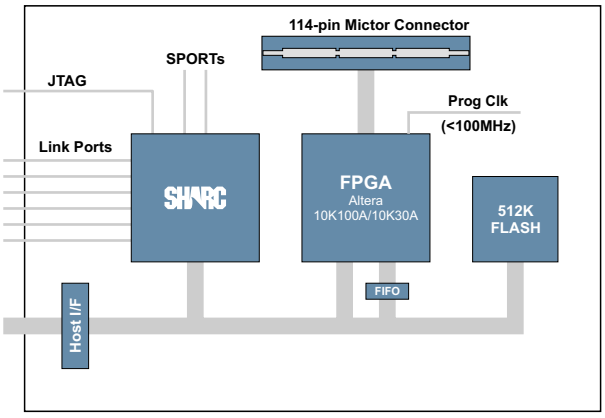
FLASH

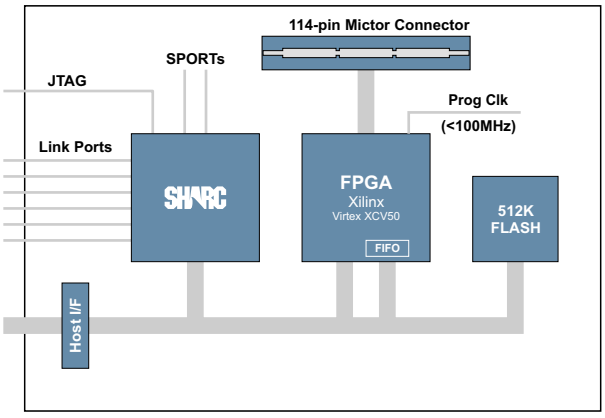
The onboard processor can read or write to 512kbytes of local FLASH memory. This permits system parameters and FPGA configurations to be stored. The FLASH memory can also be used to boot the ASP-M93 in embedded applications.

Link Ports

The ADSP-2106x DSP has six 40Mbyte/sec communication channels (link ports) which are able to operate concurrently. These link ports are designed to allow SHARCs to be inter-communicate and allow SHARC systems to be scaled and optimized for many applications. All six link ports to the SHARCPAC connectors providing a host SHARC card with full access to the ASP-M93's resources.

Block Diagram





Technical Specification

Overview

DSP Processor	ADSP-21060 or ADSP-21062

FPGA

Device	Altera 10K50E-3, 10K100A-1 or Xilinx Virtex XCV50
SHARC/FPGA Bandwidth	160Mbytes/sec
FPGA Clock	Programmable (up to 100MHz)

Digital I/O

Bits	90-bits: Altera option 50-bits: Virtex option all configurable for input or output
I/O Levels	TTL
Connectors	114-pin Mictor header (P/N 767054-3 *PdNi*)
Breakout Module	2x 40-way IDC headers (50 I/O signals)

SPORTs

Total	2 (via SHARCPAC connectors)
Bandwidth	40Mbits/sec per SPORT

Link Ports

Number	6 (via SHARCPAC connectors)
Bandwidth	40Mbytes/sec per link port

Memory

SRAM (DSP on-chip)	4Mbits (ADSP-21060), 2Mbits (ADSP-21062)
Ext FIFO (FPGA-SHARC)	32-bit x 512 (Altera only)
Ext FIFO (SHARC-FPGA)	32-bit x 512 (Altera only)
FLASH	512kbytes

SHARCPAC Interface

Host Bus Size	16-bit
Bandwidth	240Mbytes/sec
Compliance	SHARCPAC and TRANSPAC™
Size	3.1 x 4.5” (78.7 x 114.3mm)

EZ-ICE Debug Port

Connector	14-way 0.1” keyed IDC header

Software

ASP-Toolset	(*Contact Transtech for details)*

Contact Details

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