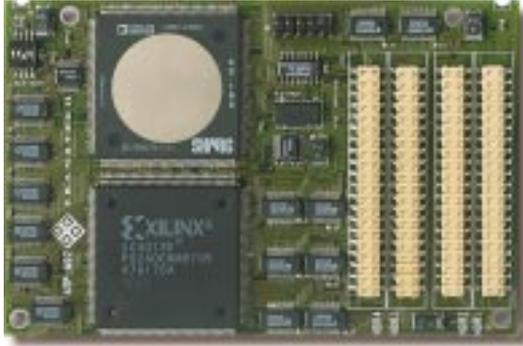


ASP-M92

Digital I/O SHARCPAC with Xilinx FPGA



- Xilinx 4013 or 4028 FPGA
- 40MHz SHARC DSP
- 100-Digital I/O pins
- FPDP option
- Programmable FPGA Clock
- 6x 40Mbyte/sec link ports
- 512kbytes FLASH
- SHARCPAC Compliant

Overview

The ASP-M92 provides high speed digital I/O to SHARC based systems at up to 160Mbytes/sec with a local Xilinx® FPGA and ADSP-2106x processor.

Coupling an FPGA with a SHARC DSP allows high speed digital I/O to be acquired and pipelined into high performance DSP arrays.

Configurable for either input or output, 100 TTL I/O channels are provided via four 40-pin headers. The I/O channels can be configured individually as bits or as groups.

The FPGA Advantage

Exploiting FPGA technology, the ASP-M92 not only allows for fully programmable digital I/O, but can also provide high speed pre-processing. This could include FFTs, digital filtering and data reduction. In combination with a Xilinx FPGA a SHARC provides a 120MFLOP DSP engine and communications ports to SHARC arrays and other host processors.

The ASP-M92 is available fitted with either a Xilinx XC4013E or XC4028EX FPGA. This offers a choice in complexity, speed and cost. Since the interface timings are handled by the FPGA, adapter modules can be very simple needing only to provide the appropriate buffering, level conversion and appropriate connector.

FLASH

The onboard processor can read or write to 512kbytes of local FLASH memory. This permits system parameters and FPGA configurations to be stored. The FLASH memory can

also be used to boot the ASP-M92 in embedded applications.

Link Ports

The ADSP-2106x DSP has six 40Mbyte/sec communication channels (link ports) which are able to operate concurrently. These link ports are designed to allow SHARCs to be inter-communicate and allow SHARC systems to be scaled and optimized for many applications. All six link ports to the SHARCPAC connectors providing a host SHARC card with full access to the ASP-M92's resources.

FPDP I/O Option

The ASP-M92 has an optional Front Panel Data Port (FPDP) adaptor. FPDP defines a simple, low cost high speed data transfer mechanism, primarily used within VME based acquisition systems. FPDP allows for 32-bit synchronous data transfers of up to 160Mbytes/sec through a multi-drop ribbon cable. FPDP can be used to connect local boards or systems making it easy to use. The ASP-M92's FPDP option comprises of an I/O adaptor kit and FPGA configuration software. FPDP can be used with an array of acquisition cards including the VGX series analog input cards from Pentland Systems.

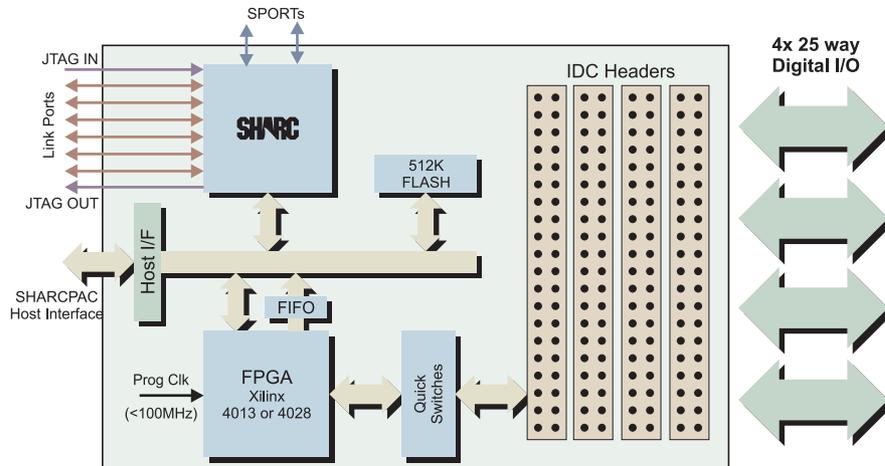
Ideal applications for ASP-M92s include:

- **High speed digital interface**
radar, digital camera, FPDP, etc.
- **Digital Signal Processing**
FFTs, FIR & IIR filters, decoders, etc.
- **Imaging**
convolutions, correlation, edge detection, translation, etc.



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Block Diagram



Technical Specification

Overview

DSP Processor	ADSP-21062 or ADSP-21060
Clock Speed	40MHz
DMA	10 channel (on-chip), 240Mbytes/sec

FPGA

Device	Xilinx XC4013E or XC4028EX
Bandwidth	160Mbytes/sec SHARC - FPGA
FPGA Clock	Programmable (up to 100MHz)

Digital I/O

Bits	100 (configurable for input or output)
I/O Levels	TTL
Connectors	4x 40-way 0.1" IDC headers (25 I/O pins per IDC header)

SPORTs

Total	2 (via SHARCPAC connectors)
TDM mode	yes
Bandwidth	40Mbits/sec per SPORT

Link Ports

Number	6 (via SHARCPAC connectors)
Bandwidth	40Mbytes/sec per link port

Memory

SRAM (DSP on-chip)	2Mbits (ADSP-21062)
FIFO (FPGA-SHARC)	32-bit x 512
FLASH	512kbytes

SHARCPAC Interface

Host Bus Size	16-bit
Bandwidth	240Mbytes/sec
Compliance	SHARCPAC and TRANSPAC™
Size	3.1 x 4.5" (78.7 x 114.3mm)

Power

Typical	8.5W
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Software

ASP Toolset, Virtuoso, 21K DSP libraries, Mountain-ICE and EZ-ICE
Contact Transtech for further details of software support

Contact Details

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