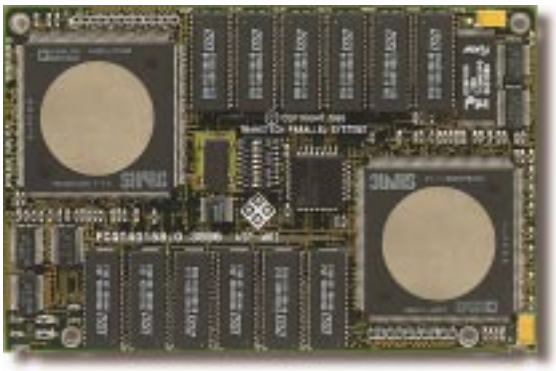
ASP-M62

Twin SHARC SHARCPAC with SRAM



- 2 ADSP-2106x DSPs
- Cluster/non-clustered opton
- 2/3Mbytes SRAM
- 8x 40Mbyte/sec link ports
- JTAG debug support
- 512kbytes FLASH
- TRANSPAC compliant
- SHARCPAC compliant

Overview

The ASP-M62 is a SHARCPAC with 2 Analog Devices ADSP-2106x SHARCs each with up to 1.5Mbytes of zero wait state SRAM. The ASP-M62 high speed architecture is suited to memory intensive computation and data distribution tasks in signal processing.

SHARC Bus Coupler

Transtech's unique switch selectable Bus Coupler allows the SHARCs to operate as a cluster, or independently. Cluster operation is ideal when the application calls for shared data and/or on-chip resources, but this shares bus bandwidth between processors. Independent operation provides full memory bandwidth to each SHARC's memory bank simultaneously.

SRAM

As standard, the ASP-M62 is fitted with 3Mbytes SRAM. The board can also be supplied with up to 3Mbytes (48-bits wide) for boards with ADSP-21062 devices, 2Mbytes (32-bits wide) for ADSP-21060 boards.

FLASH

The onboard processor can read or write to 512kbytes of local FLASH memory. This permits system parameters to be stored. The FLASH memory can also be used to boot the ASP-M62 in embedded applications.

Link Ports

The ASP-M58 has fourteen 40Mbyte/sec communication channels (link ports) which are able to operate concurrently. These link ports are designed to allow SHARCs to be inter-communicate and allow SHARC systems to be scaled and optimized for many applications.

Host Bus Interface

The root SHARC supports a 16 bit host bus. This allows a system processor (such as the Pentium in a PC environment via a VME, ISA or PCI gateway) to access the IOP of the root SHARC, via the host board. The root SHARC can be booted from this bus.

Debugging

The ASP-M62 incorporates an EZ-ICE/ Mountain-ICE header to provides in-circuit emulation via JTAG. To use this facility, an EZ-ICE emulator and PC-add-in card (available separately) is required. This provides the basis for a complete development and debug environment. Using EZ-ICE allows C-source level debugging within a user-friendly GUI interface and complete control over loading, execution and inspection of program variables.

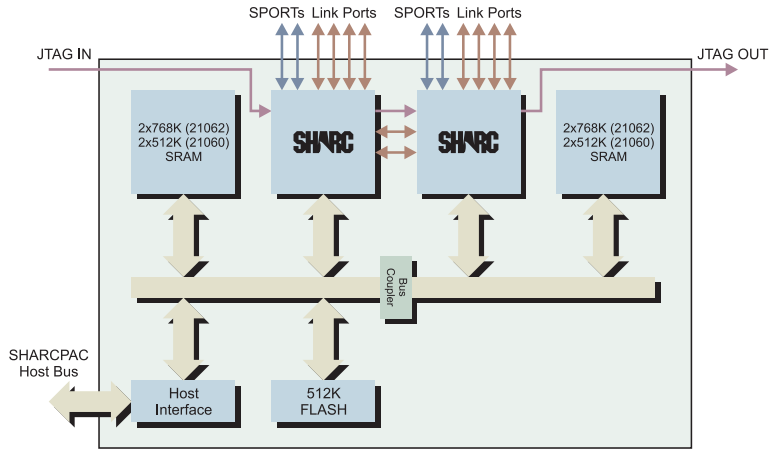
Software Support

Software support includes Transtech's ASP Toolset and a wide range of 3rd party products such as Virtuoso™.

TRANSTECH DSP

www.transtech-dsp.com

Block Diagram



Technical Specification

Processor

Type	ADSP-21062 or ADSP-21060
Number	2
Clock speed	40MHz

Memory

SRAM	2x128kx48 per DSP (ADS21062) 2x128kx32 per DSP (ADS21060)
FLASH	512kx8bit

Internal Link Ports

Architecture	Pipeline
Bandwidth	40Mbytes/sec

External Links Ports

Number	8
Bandwidth	40Mbytes/sec
Connector	As per SHARCPAC specification

Debug Port

EZ-ICE via SHARCPAC connector

SPORTs

Number	4 - 2 per processor, routed via SHARCPAC connector

Power Requirement

Typical	17.5W (2 processor)

Software Support

ASP Toolset, Virtuoso, 21K DSP libraries, Mountain-ICE and EZ-ICE
Contact Transtech for further details of software support

Contact Details

Transtech DSP
20 Thornwood Drive, Ithaca, NY 14850-1263, USA
Tel: 607 257 8678 Fax: 607 257 8679
email: sales@transtech-dsp.com

Transtech DSP
19 Manor Courtyard, Hughenden Avenue, High Wycombe, HP13 5RE, UK
Tel: +44(0)1494 464432 Fax: +44(0)1494 464472
email: sales@transtech-dsp.com

www.transtech-dsp.com