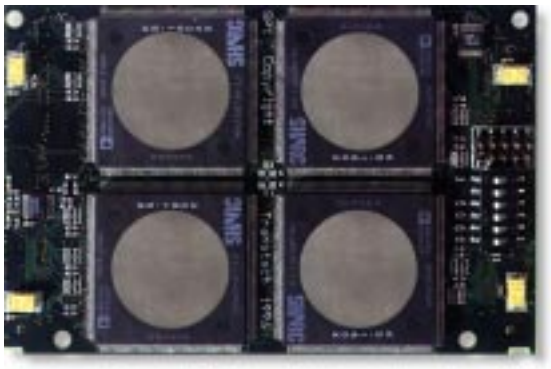
ASP-M54

Quad SHARC SHARCPAC



- 2 or 4 ADSP-2106x DSPs
- Cluster architecture
- 10x 40Mbyte/sec link ports
- 4x 40Mbit/sec SPORTs
- JTAG debug support
- 512kbytes FLASH
- TRANSPAC compliant
- SHARCPAC compliant

Overview

The ASP-M54 is a quad clustered ADSP-2106x DSP SHARCPAC. With 10 external 40Mbyte/sec link port connections, the ASP-M54 is suited to computation and data distribution tasks in signal processing and other applications.

Cluster operation for all SHARC devices is used. This allows any SHARC to share on-chip resources with all other SHARCs in the cluster.

FLASH

The onboard processor can read or write to 512kbytes of local FLASH memory. This permits system configurations to be stored. The FLASH memory can also be used to boot the ASP-M54 in embedded applications.

Link Ports

The ASP-M54 has ten 40Mbyte/sec communication channels (link ports) which are able to operate concurrently. These link ports are designed to allow SHARCs to be inter-communicate and allow SHARC systems to be scaled and optimized for many applications.

Host Bus Interface

The root SHARC supports a 16 bit host bus. This allows a system processor (such as the Pentium in a PC environment via a VME, ISA or PCI gateway) to access the IOP of the root SHARC via the host board. The root SHARC can be booted from this bus.

Debugging

The ASP-M54 incorporates an EZ-ICE/ Mountain-ICE header to provides in-circuit emulation via JTAG. To use this facility, an EZ-ICE emulator and PC-add-in card (available separately) is required. This provides the basis for a complete development and debug environment. Using EZ-ICE allows C-source level debugging within a user-friendly GUI interface and complete control over loading, execution and inspection of program variables.

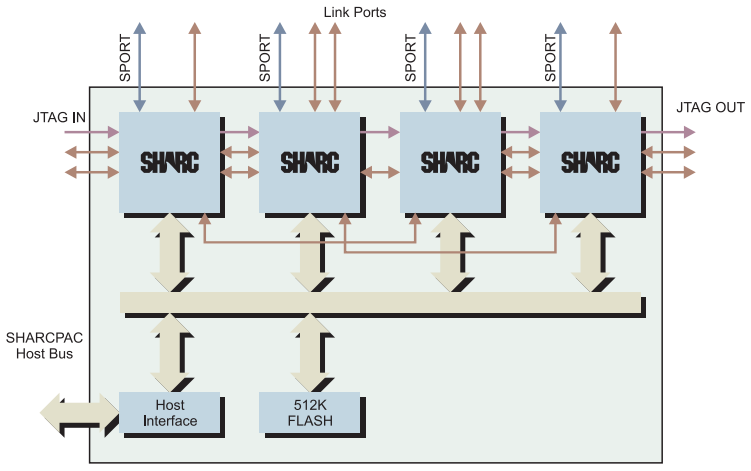
Software Support

Software support includes Transtech's ASP Toolset and a wide range of 3rd party products such as Virtuoso™.

TRANSTECH DSP

www.transtech-dsp.com

Block Diagram



Technical Specification

Processor

Type	ADSP-21062 or ADSP-21060
Number	4
Clock speed	40MHz

Memory

FLASH	512kx8bit

Internal Link Ports

Architecture	Pipeline
Bandwidth	40Mbytes/sec

External Links Ports

Number	10
Bandwidth	40Mbytes/sec
Connector	as per SHARCPAC specification

Debug Port

EZ-ICE/Mountain-ICE via SHARCPAC connector

SPORTs

Number	4 - via SHARCPAC connector

Power Requirement

Typical	11W (4 processor)

Software Support

ASP Toolset, Virtuoso, 21K DSP libraries, Mountain-ICE and EZ-ICE
Contact Transtech for further details of software support

Contact Details

Transtech DSP
20 Thornwood Drive, Ithaca, NY 14850-1263, USA
Tel: 607 257 8678 Fax: 607 257 8679
email: sales@transtech-dsp.com

Transtech DSP
19 Manor Courtyard, Hughenden Avenue, High Wycombe, HP13 5RE, UK
Tel: +44(0)1494 464432 Fax: +44(0)1494 464472
email: sales@transtech-dsp.com

www.transtech-dsp.com