TVG5

Dual PowerPC™ 7455/57 VME Embedded Processing Systems

Features

Dual MPC7455/57 with AltiVec™ @ 1300MHz+

Independent processor nodes

Up to 1Gbytes DDR SDRAM (ECC) per node

Cache Memory: 64KB L1; 512KB L2; 2MB L3

Up to 128MBytes Flash per node

PCI over P0

Three independent 64-bit PCI busses

Two PMC slots

2 Gigabit Ethernet ports

The TVG5 is a member of Transtech's Pegasus family of embedded PowerPC processing systems and features the power of the latest AltiVec PowerPC processors: ideal for intensive signal processing applications.

The Pegasus philosophy is based around an integrated, modular approach to I/O and processor enhancements utilizing PMC I/O, PowerPC, DSP and FPGA modules offering the system designer a huge array of options when contemplating the best system approach for the application while reducing the development time.

TRANSTECH™ DSP

www.transtech-dsp.com

Dual Processor - MPC7455/57

- Scaleable processor power from 800-1300MHz +
- Node A/B: 7455/57 PowerPC with AltiVec technology
- Contact Transtech DSP for latest CPU version
- High efficiency onboard switching regulator (DC/DC)
- Fanless cooling with heatsink

Cache

	Level 1	*Level 2*	*Level 3*
Node A/B 7455	32+32 kB	256 kB	1/2 MB
Node A/B 7457	32+32 kB	512 kB	1/2 MB

Memory - DDR SDRAM

- 256MB to 1 GB, 72-bit wide with error correction (ECC) for each processor node
- Rugged design with baseboard soldered chips

Flash (Boot ROM Integrated)

- Up to 128MB, 32-bit wide, high speed for processor node 1
- Up to 128MB, 32-bit wide, high speed for processor node 2
- Boot device select for node A/B (Bank 1 of 2)
- Hardware write protection
- Rugged design with baseboard soldered chips

Non Volatile Memory

- 3 X 8 kB non volatile memory realized with serial EEPROM

Dual Marvell MV-64360 each with:

- 133MHz, 64-bit wide system bus
- Two 64-bit wide PCI busses (PCI 2.2/PCI-X) (33/66 133MHz)
- 32-bit up to 133MHz device bus for Flash, RTC, I/O
- 512 byte posted write and 512 byte read buffer for unlimited DMA bursts between PCI busses and main memory
- 4X DMA controllers for memory and PCIbus transfers
- 4X 32-bit timer/counter for system timing or periodic interrupts
- I2O intelligent I/O support with message and doorbell registers
- 2 Mbit SRAM

VME64 - Tundra Universe IID

- Industry standard *CA91C142D* PCI to VME controller
- 60-70 MB/S transfer rate, full VME system controller
- FIFO write posting, DMA controller w/ linked list support
- Master/slave transfer modes: BLT, ADOH, RMW, LOCK, RETRY
- A32/A24/A16 and D64(MBLT)/D32/D16/D8
- Geographical addressing

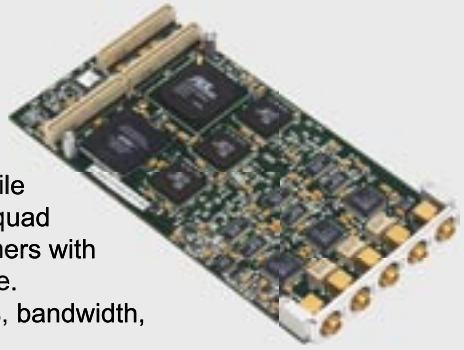
Ethernet - Marvell MV-64360

- Two integrated Ethernet controllers per chipset, connected via internal crossbar (main memory, PCI busses, DMA controllers)
- Two Gigabit Ethernet ports: 10/100/1000Mbit/s auto-negotiation interface
- Two fast Ethernet ports: 10/100Mbit/s auto-negotiation interface
- Ready for AFDX
- Two Gigabit channels available at P0 rear I/O
- Two 10/100Mbit channels at P0 rear I/O or one front I/O

Dual PMC Extension Slot - IEEE P1386/1386.1

- PMC1 64-bit/33MHz, 66MHz and full rear I/O at P0 (PCI or PCI-X)

Analog I/O

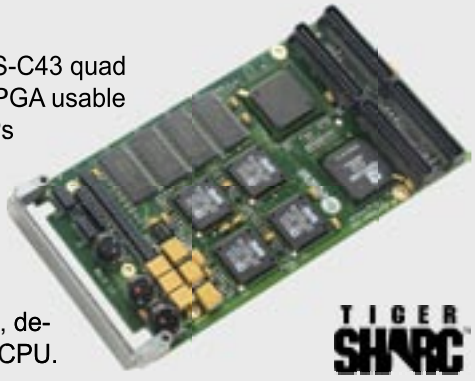


PMC adapters offer broad diversity in analog I/O, from simple analog to digital conversion to multi-channel digital receivers and ideal for applications including software defined radio and radar.

The ECDR-GC314-PMC, shown here, accepts three analog inputs with IFs of up to 100MHz utilizing 14-bit, 80MHz AD6645 converters, while maintaining an SFDR in excess of 90dBFS. Industry standard GC4016 quad downconverters receive this data via a crossbar switch, providing designers with twelve digital receiver channels output to the 64-bit, 66MHz PCI interface.

Other PMC modules are available with different numbers of channels, bandwidth, digital receivers as well as analog outputs.

TigerSHARC DSP Sub-system



PMC modules to augment the processing power of the TVG5 include the TS-C43 quad TigerSHARC DSP board featuring 7.2GFLOPS performance plus a large FPGA usable as a co-processor and flexible digital I/O port. The use of TigerSHARC DSPs provides scalable DSP sub-system with low power consumption.

The FPGA provides two 64-bit datapaths independent of the 64-bit, 66MHz PCI interface and of each other. It also shares the high bandwidth local bus with the TigerSHARC DSPs providing it full access to the board's many resources.

The TS-C43 ideally used as a front-end processor (FFTs, de-modulation, de-coding, etc.) due to its direct data I/O prior to passing data to the PowerPC CPU.

- PMC2 64-bit/33MHz and full rear I/O at P0
- Ready for PCI over P0
- Supports ccPMC draft standard VITA 20-200x with N-style

High Speed Serial I/O - RS-232/422/485

- Four multi protocol serial controllers (MPSC) MV64360 up to 10Mbit each
- HDLC, BiSync, FM0/1, UART, transparent protocols NRZ, NRZ1, FM0/1, Manchester, differential Manchester
- Dedicated DPLLs for clock recovery and data encoding
- Three internal Baud rate generators or external clocks
- RxD, TxD, RTS, CTS, CD, TxClk (in/out), RxClk (in/out)

Front Panel and Rear I/O (Transition Module VG5TM)

- PMC I/O slot 1 with full rear I/O support or partial configuration with serial ATA feature
- PMC I/O slot 2 available in full or partial configuration

Function	*Full PMC2-I/O*	*Partly PMC2-I/O*	*Front Panel I/O*
COM 1	Yes	Yes	Yes
COM 2	Yes	Yes	Yes*
COM 3 to 6	Yes	Yes	-
Gigabit Eth. Ch 1	Yes	Yes	Yes*
Fast Eth. Ch 2	Yes*2	Yes*2	Yes*2
Gigabit Eth. Ch 3	Yes	Yes	-
Fast Eth. Ch 4	Yes	Yes	-
PMC 1	64-pin	64-pin	Yes
PMC2	64-pin	-	Yes
Reset	Yes	Yes	-
Watchdog	-	Yes	-
BootSel	Yes	Yes	-
CardFail	Yes	Yes	LED
UserLED	-	-	LED
COP node A/B	-	Yes	-
GPIO	-	Yes	-

* NOTE: PMC slot 2 not available with optional front I/O
*2 Front or Rear I/O

With a large array of I/O paths, the TVG5 offers extensive choices when it comes to analog data input, the augmentation of the board's processing power and implementation of various industry standard or custom digital I/O protocols. A wide variety of supported PMC modules, each utilizing both PCI and user I/O data paths offers developers the ability to rapidly put together a high bandwidth, semi-custom processing system using tried and tested COTS boards.

Environmental Specifications

Temperature - (Except N-Style)

- Highest reachable operating temperature depends on processor type, speed and ambient conditions (airflow)
- All values under typical conditions w/o PMC module

	Operating	Storage
Standard	0°C to +70°C	-40°C to +85°C
Extended	-40°C to +85°C (TBC)	-40°C to +85°C

Temperature - (N-Style)

- Highest reachable operating temperature depends on processor type, speed and card edge temperature
- All values under typical conditions w/o ccPMC module

	Operating	Storage
Extended	-40°C to +85°C	-55°C to +105°C

Humidity

- Operating 5 - 95% @ 40°C
- Storage 5 - 95% @ 40°C
- Non condensing

Altitude

- Operating 15,000 ft. (4.5 km)
- Storage 40,000 ft. (12 km)
- Vacuum for conduction cooled board

Shock

- C, I Style 12g/6 rms, 3 axis, up & down, 5 hits/direction
- R Style 20g/6 rms, 3 axis, up & down, 5 hits/direction
- N Style 100g/6 rms, 40g/11 ms, 3 axis, up & down, 5 hits/direction

Vibration

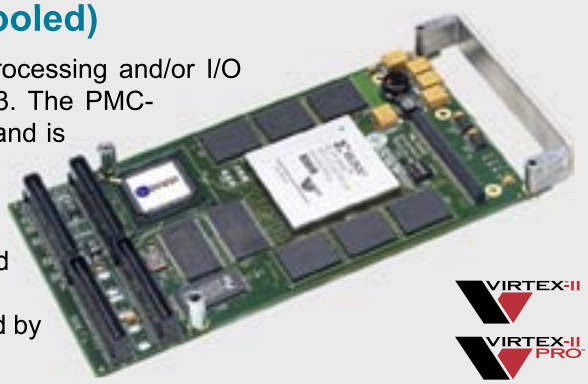
- C, I Style 2g rms @ 5 to 100 Hz, 30 minutes each axis
- R Style 2g rms @ 5 to 2000 Hz, 30 minutes each axis
- N Style 14g rms @ 5 to 2000 Hz, 30 minutes each axis

Front Panel	C	I	R	N
Front Panel	●	●	●	-
Front stiffener	-	-	-	●
Middle stiffner	-	-	●	●
Wedge locks	-	-	-	●
Parts soldered	●	●	●	●
Extended Temperature	-	●	●	●
Conformal coating	-	-	●	●
Conduction cooled	-	-	-	●

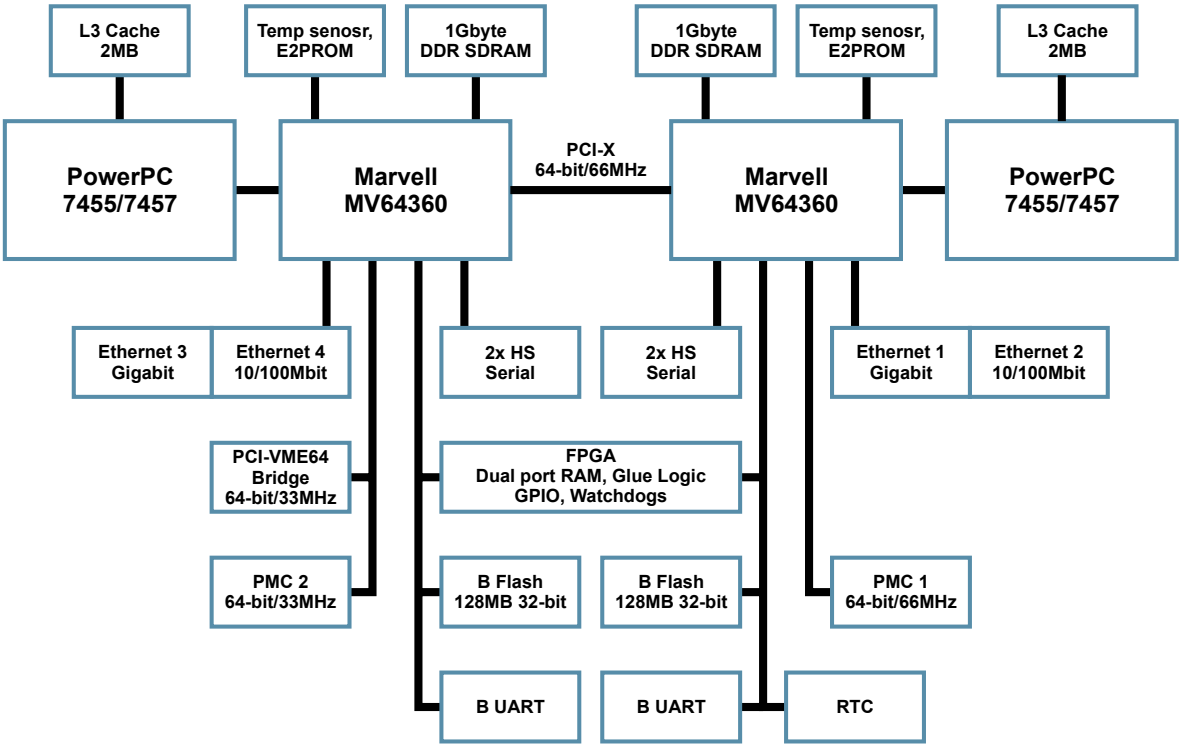
FPGA Acceleration & I/O (Rugged & Air-cooled)

The reconfigurable power of FPGAs to implement custom processing and/or I/O can be achieved using the PMC-FPGA02 and PMC-FPGA03. The PMC-FPGA02 features a Virtex-II FPGA with up to 8 million gates and is complemented by high speed QDR SRAM. Front panel and PMC user I/O is supported, independent of the 64-bit, 66MHz PCI interface. The PMC-FPGA03 offers a similar architecture, but features a Virtex-II Pro FPGA and a rugged/conduction-cooled build variant.

Custom I/O adapter modules and firmware may be generated by users, though standard adapters and IP cores are available.



Block Diagram



Technical Specification Summary

General

Number of Processor Nodes	2
Each Node:	PowerPC + PMC + Memory + Inter-node communications + PCI fabric

Inter-Node Communications

PCI-X bus	64-bit/66MHz
FPGA	Dual Port RAM

Processors

Number	2
Device	7455/57 PowerPC
Speed	800 to 1300MHz +
Cache (on chip)	7455 - 32 + 32KB L1; 256KB L2 7457- 32 + 32KB L1; 512KB L2

Memory

SDRAM	Up to 1Gbyte ECC DDR per node
FLASH	128Mbytes per node Boot ROM integrated Hardware write protection
Cache	2Mbytes L3

Mechanical

Board Format	6U VME (single slot)

PCI

Device	Marvell MV-64360 bridge
Compliance	2x 64-bit PCI 2.2 buses 64-bit, 66MHz PCI-X interconnect 64-bit, 133MHz system bus I^2O + Master/slave/DMA
Enhancements	PCI via P0
Bandwidth	>500Mbytes/sec

Power

TBA

Software Support

Operating System	VxWorks, Linux
Utilities	Yes
Example code	Yes

Debugging

JTAG interface	Onboard and rear I/O
COP interface	For external emulator

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