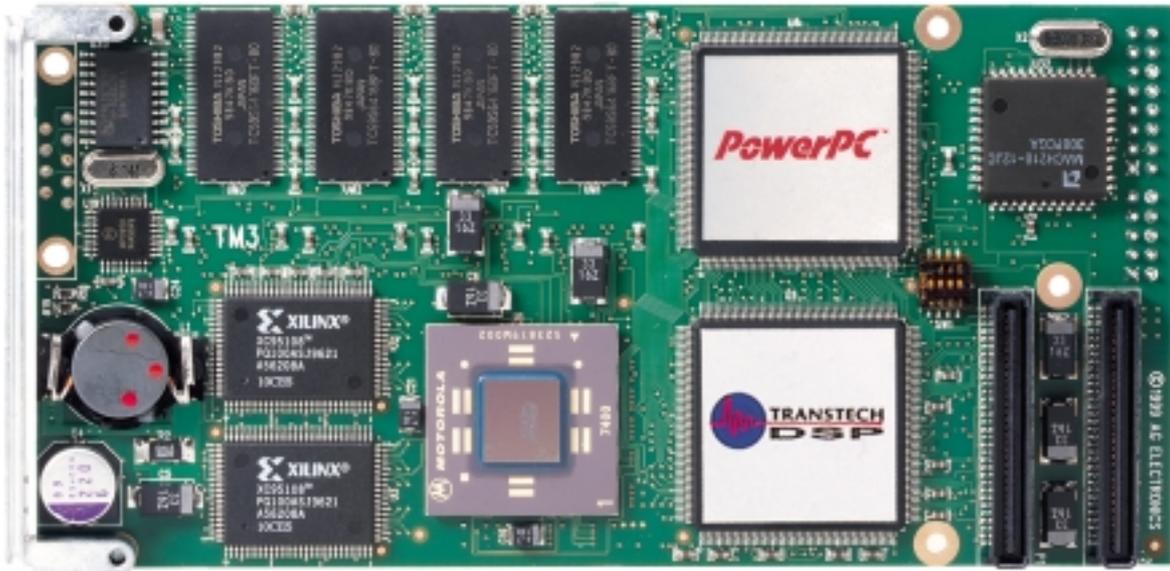


TM3

PowerPC 750/7400 PMC Module



Features

- PowerPC 750 (G3) or 7400 (G4) CPU
- 1 or 2Mbytes L2 Cache
- Upt o 256Mbytes SDRAM
- 512Kbytes FLASH
- 132Mbytes/sec PCI (32-bit/33MHz rev 2.1)
- Bundled GNU Tools & Utilities
- VxWorks™ BSP
- PowerPC Linux Support
- Support AMC PowerTAP JTAG Emulator

Aimed at high performance, embedded applications, the TM3 is a high performance processor module based on the latest PowerPC processor with up to 256Mbytes SDRAM. The TM3 removes otherwise redundant system I/O such as networking to provide a processor node that is both fast and efficient. To support this, the TM3 also includes fast DMA engines to move data quickly between other nodes or the host system.

Able to be used on its own, or as part of a multiprocessing system, the TM3 is ideal for embedded applications including DSP, imaging, computer telephony and transaction processing.



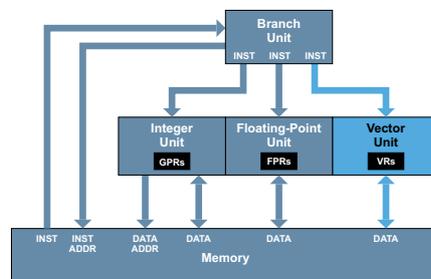
www.transtech-dsp.com

PowerPC 7400 with AltiVec™

The PowerPC 7400 is the latest member of the PowerPC processor family and continues to provide a highly advanced superscalar architecture to deliver very high integer and floating-point performance.

A major feature of the PowerPC 7400 processor is the addition of a 128-bit vector processing unit. This is otherwise known as the AltiVec extension and operates in a SIMD mode (Single Instruction Multi-Data). See *Figure 1* for an overview. With AltiVec, the PowerPC can accelerate many DSP and multimedia type applications by being able to achieve anything up to 20 operations in a single CPU clock cycle. As an example, the vector unit can process 16x 8-bit data elements in parallel. The vector unit can handle parallel data elements of other lengths including floating-point. See *Table 1* and *Figure 2* for summaries.

With the new vector unit come 162 new instructions. These are similar to those found on the scalar units, but in SIMD format. To implement these instructions at a high level, C language extensions have been made available. Using



PowerPC 7400 architecture overview with AltiVec™ vector unit
Figure 1

language extensions, rather than relying on compiler efficiencies, permits maximum performance to be achievable.

Through the AltiVec Instruction Set Architecture many application segments are supported including Voice over IP (VoIP), speech recognition, voice/sound processing and communications including multi-channel modems, software modems, data encryption. The parallel nature of AltiVec means that PowerPC 7400 can replace modem banks with a single processor whereas many were previously needed. This simplicity makes development easier and reduces cost.

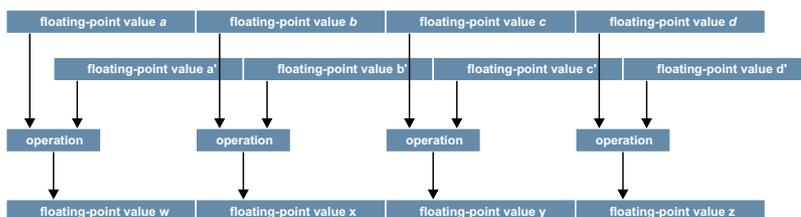


PowerPC 7400 Summary Specification

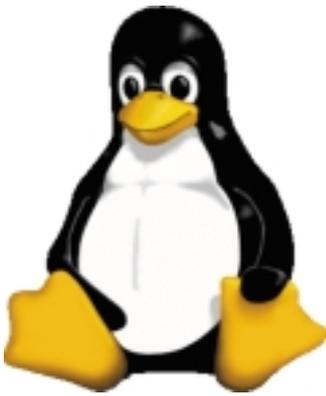
- **Internal CPU Speeds**
350, 400 and 450MHz
- **Bus Interface**
64-bit bus with MPX/60x protocol
- **Cache**
L1: 32Kbyte instr + 32Kbyte data
L2: up to 2Mbytes
- **Power Consumption**
5W (typ)/11.5W (max)
- **Package**
360 ball CBGA
- **Benchmark Estimates (450MHz)**
21.4 SPECint95
20.4 SPECfp95
825 MIPS
- **Execution Units**
integer (2), floating-point, vector, branch, load/store, system

# Parallel Vector Operations	Data Types Supported
16-way	8-bit signed & unsigned ints and chars
8-way	16-bit signed & unsigned ints
4-way	32-bit signed & unsigned ints and IEEE floating-point numbers

Parallelism with AltiVec technology execution unit
Table 1



Parallel floating-point operations with AltiVec
Figure 2



Software Tools and Utilities Summary

- **Linux for PowerPC**
Version 2.2
- **VxWorks**
Bundled BSP
- **TCP/IP Communications**
TCP/IP across PCI for fast inter-processor communications
- **Choice for Host Programming Support**
Windows NT, Linux, DOS and Windows 95/98
- **GNU C Cross Compiler**
with run-time support
- **PowerTAP™ Adaptor**
Compatible with full In-Circuit Emulator (ICE)

Overview

The TM3 is provided with a choice of PowerPC 750 or PowerPC 7400 CPUs at different speed grades (and higher speed parts as they become available).

To achieve maximum performance, the TM3 includes a 1 or 2Mbyte L2 cache option (PowerPC 750 1Mbyte only) and uses pipeline burst SRAMs. These are connected to the CPU by a dedicated backside bus running at between 150 and 200MHz, depending on the core speed.

The CPU is connected to the SDRAM memory by an optimised for low latency and high bandwidth data streaming.

PCI Interface

The TM3 PCI interface is a PCI 2.1 compliant initiator and target. This includes the ability to generate and respond to configuration cycles.

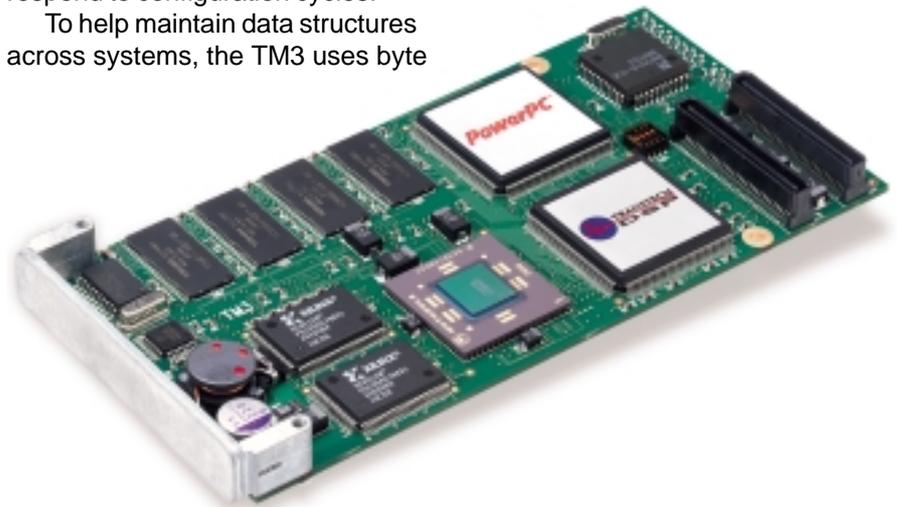
To help maintain data structures across systems, the TM3 uses byte

transfers by improving system flow control. The result is an efficient PCI interface capable of sustaining 120Mbytes/sec to and from SDRAM. Full support for scatter/gather and unaligned transfers is also included. As an initiator, the TM3 allows the CPU and DMA engines to directly access other devices.

Peripherals

The TM3 includes all the necessary resources required by leading real-time operating system such as a flash BIOS ROM for boot firmware, non-volatile memory, a timer and a serial port. The serial port is available through a 9-way D-type connector, and provides an invaluable resource for operating systems to implement diagnostics or configuration support.

Utilities are supplied to test and program the BIOS and NVRAM, as well as programming examples for the timer and serial port.



invariant addressing and hardware endian-conversion. Also included is a pair of DMA engines with bus mastering ability. This powerful combination allows for high performance data transfers without the CPU needing to re-manipulate the data.

As a PCI target, all the TM3's on board resources are visible. This allows the host and other PCI initiators access the TM3's SDRAM, peripherals and control registers.

As part of the PCI interface, the TM3 has deep FIFO buffers. The effect of this is to smooth out burst

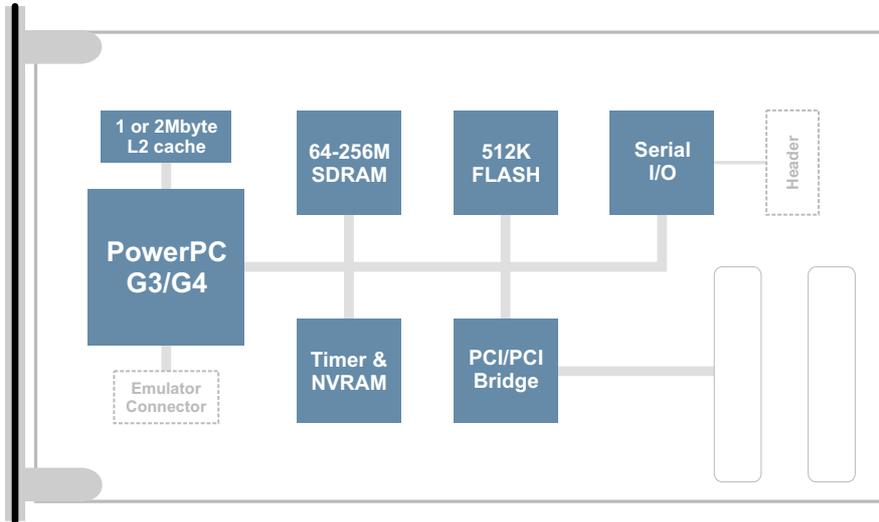
Development Tools

The TM3 includes a JTAG TAP socket and adapter that is compatible with AMC's PowerTAP™ debugger. This is functionally similar to a full in-circuit emulator.

The TM3 is bundled with a CD containing PowerPC resources and tools including:

- GNU C cross compiler for Win32 and Linux hosts
- Host drivers, libraries and utilities for Windows 95/98, Windows NT, Linux and DOS
- PCI programming examples and libraries

Block Diagram



Technical Specification

Processor

CPU	PowerPC 750 (G3): 366, 400MHz PowerPC 7400 (G4): 333, 400MHz
L1 cache (on-chip)	32kbyte instruction, 32kbyte data
L2 cache	1Mbyte PDSRAM, 133-200MHz

Memory

Type	SDRAM
Size	64/128/256 Mbytes
Bus width	64 bit
Bus speed	66 MHz
Bursting	4-1-1-1-2-1-1-1
FLASH	512Kbytes

PCI Interface

Compliance	PCI 2.1
Width	32 bit
Voltage keying	5V
Speed	33 MHz
Bandwidth	132Mbytes/sec

Serial Port

Ports	1
Connector	9-way D-type (PC pin-out)
Baud rate (max)	128K; (9600, no parity, stop - def)
I/O Device	16550 compatible

Mechanical

Board form factor	IEEE P1386.1 single width PMC
Weight	115 g

Environmental

Power dissipation	TBA
Operating temperature	0 to 65°C
Storage temperature	-15 to 85°C

Software

Resources CD-ROM	GNU C cross compiler, libraries, examples and host utilities for Windows 95/98 and Windows NT
Operating Systems	VxWorks, PowerPC Linux 2.2

Ordering Information

TM3-s-m	PowerPC™ G3 with 1MByte L2 cache
TM3A-s-m	PowerPC™ G4 with 1MByte L2 cache
TM3A2-s-m	PowerPC™ G4 with 2MByte L2 cache

where **s**: processor clock (MHz) - 333, 366, 400 **m**: memory (MBytes) - 64, 128, 256

example: *TM3A2-400-128* 400MHz PowerPC G4 with 2Mbytes L2 cache and 128Mbytes memory

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