

Pegasus

PowerPC System Solutions



www.transtech-dsp.com

Pegasus PowerPC

Features

- PowerPC 7455/57 CPUs
- TigerSHARC DSP sub-systems
- Embedded Xilinx Virtex-II and Virtex-II Pro FPGAs
- Modular input/output based on open standards
- VxWorks, Linux, Geda environments (call for availability)
- Support software (libraries, drivers, utilities, examples) (call for availability)
- Systems integration service
- Open Standards

Benefits

- Industry standard processor family
- Extensive code base
- Wide support
- High performance
- Optimal front-end data processing with balanced I/O
- Deterministic operation
- No-compromise performance, often the only way to achieve performance goals
- Reduced bottlenecks when used for front-end processing
- Wide range of IP cores
- Access to wide range of I/O including, digital receivers, analog I/O, graphics and, networking
- Wide range of applications using common building blocks
- Optimal tools for given applications
- Heterogeneous development option (Geda)
- Choice of tools
- Simplified code development
- Optimal performance
- Accelerated time-to-market
- Free up engineering time to focus on the application itself
- Access to signal processing hardware specialists
- Highly configurable
- Expandable
- Application portability

Pegasus System Overview

The Pegasus family of sub-system components from Transtech DSP is aimed at a range of high-performance applications including software radio, radar, sonar and signal intelligence; ranging from commercial air-cooled to rugged conduction-cooled builds. Pegasus includes 'state-of-the-art' components such as PowerPC CPUs, DSP-sub-systems, FPGA co-processors, analog and digital I/O and software. This is achieved through a combination of Commercial Off-The-Shelf (COTS) equipment, coherent applications engineering and a bespoke design service (where existing components or interfaces do not already exist).

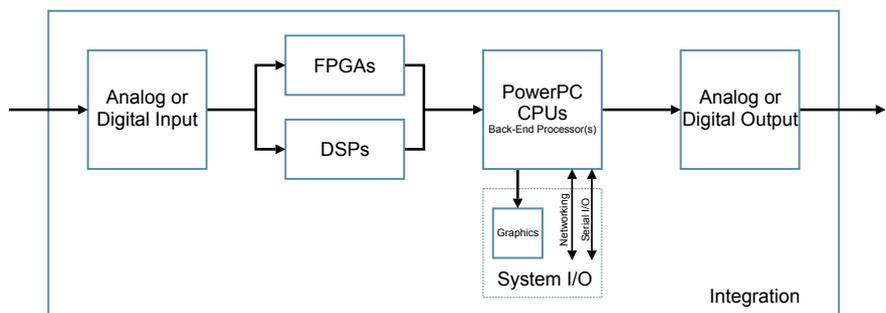
To compliment Transtech DSP's expertise in processor sub-systems, we have forged strong relationships with specialists in fields such as high-speed analog I/O, development tools and FPGA IP cores. The effect is one of providing flexible and tailored sub-systems from a single source of supply, responsibility and support. This simplifies the overall project design and development cycle by allowing our customers to focus on their key areas of expertise and not needing to concern themselves with issues such as, 'is the driver compatible' or 'do I need certain cables', etc.



TVG5 PowerPC CPU Cards for Scalable Performance

The philosophy behind Pegasus is to use COTS equipment backed up by a coherent integration service from Transtech to remove the risk and ensure that the details are 'taken care of'.

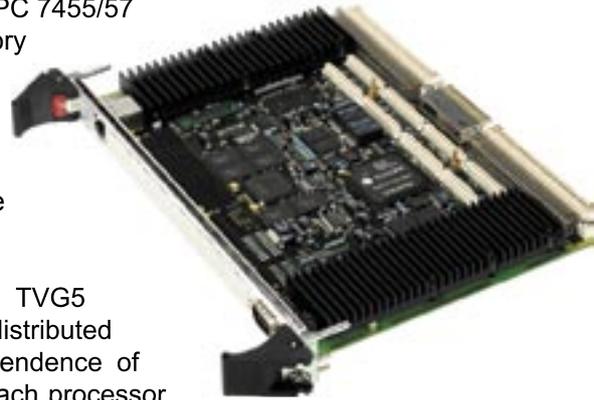
Pegasus Pentium systems are also available. Call Transtech for more information.



Overview of a Pegasus PowerPC System

PowerPC

At the heart of a Pegasus PowerPC sub-system are one or more PowerPC CPUs within a VME framework. Based on a TVG5, a Pegasus system employs a latest generation PowerPC 7455/57 CPU with a fast bridge to both memory and I/O data streams. An industry standard embedded CPU able to run a wide variety of operating systems; the PowerPC is a well supported device suitable for a wide range of applications.

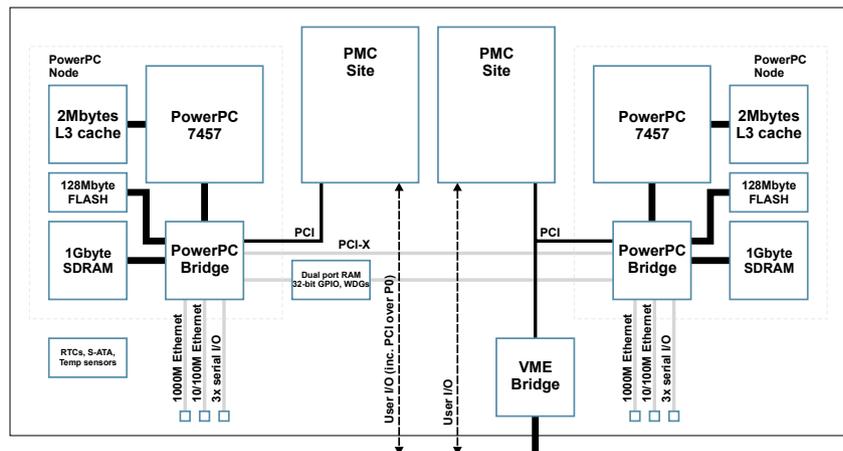


Key to the performance of the TVG5 PowerPC processor cards is a fully distributed processor architecture. The independence of the processor nodes means that each processor does not have to share bandwidth with the other and increases overall system performance. Also included are high-speed data I/O via PCI to two PMC sites for I/O expansion and numerous system resources such as multi-channel Gbps Ethernet and serial I/O channels.

TVG5

- 2x PowerPC 7455/57 CPUs - independent nodes/fully distributed architecture.
- Up to 1Gbyte ECC DDR DRAM per PowerPC
- 2x PMC site for local I/O and co-processor expansion
- 2x Gigabit Ethernet ports
- Up to 128Mbytes Flash per node
- Commercial/air-cooled to rugged/conduction-cooled variants
- VME format

PowerPC Processor Card

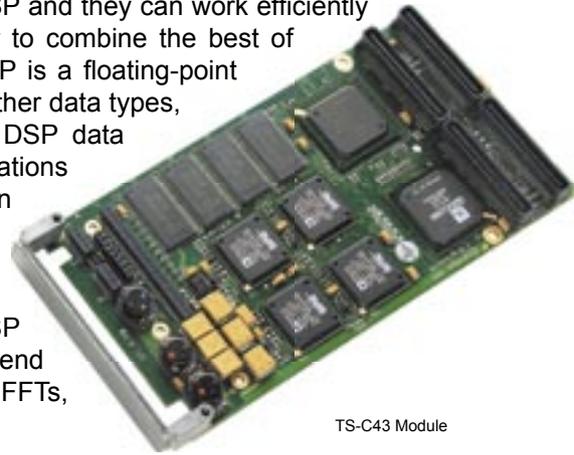


Dual PowerPC Node based on TVG5 SBC

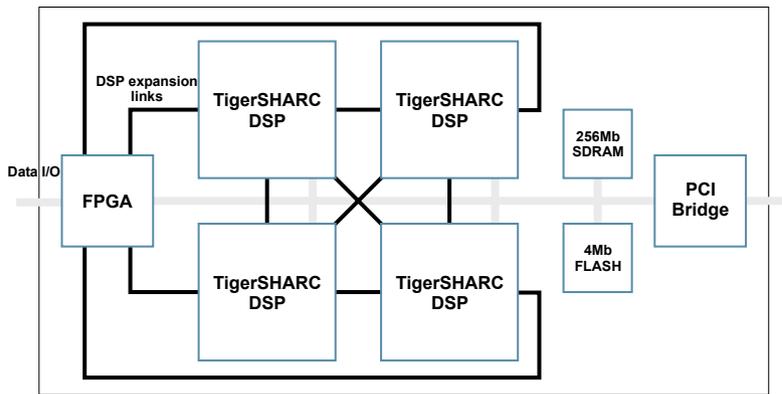
DSP Sub-System

The PowerPC CPU is good at DSP type operations, but there are times when an actual DSP is required. This is often the case when predictable [low latency and deterministic] operation with sustained datastreams is important in applications such as radar, sonar or telecommunications. This is because DSPs are optimized for balanced input/output and processing ability i.e. no data bottlenecks, but high-performance. This balanced architecture is the key advantage of DSPs. For example, a 300MHz TigerSHARC DSP has 1800Mbytes/sec I/O bandwidth and 1800MFLOPs of performance whereas an 8000MFLOP PowerPC/AltiVec has a bandwidth of a little over 1Gbyte/sec and is bandwidth limited. Consequently, a PowerPC CPU is less effective if the class of operation requires high sustained data throughput. DSPs such as the TigerSHARC DSP also have the ability to scale by easily adding additional DSPs and offer high performance at low power - especially where space is a premium.

Within the Pegasus family are DSP cards based on Analog Devices' ADSP-TS101, the TigerSHARC DSP and they can work efficiently alongside the PowerPC processor to combine the best of both worlds. The TigerSHARC DSP is a floating-point DSP, equally capable processing other data types, with four 200Mbytes/sec DSP to DSP data links for point-to-point communications with other TigerSHARC DSPs - an efficient way achieve multi-DSP solutions. These link ports are in addition to its main processor bus. This all makes the TigerSHARC DSP (or array of DSPs) good for front-end data processing for such tasks as FFTs, digital filters, correlations, etc.



TS-C43 Module



TS-C43 Overview

The use of DSP modules within these systems is usually to fulfill a front-end processing requirement. Since the data rates can be high, the DSPs need to be closely coupled with the I/O data streams. Local FPGAs have been added for just this purpose: FPGA can be used to directly interface to the 'outside world'. All of this allows the PowerPC to receive pre-processed data, from the DSPs, and without introducing data bottlenecks unnecessarily.

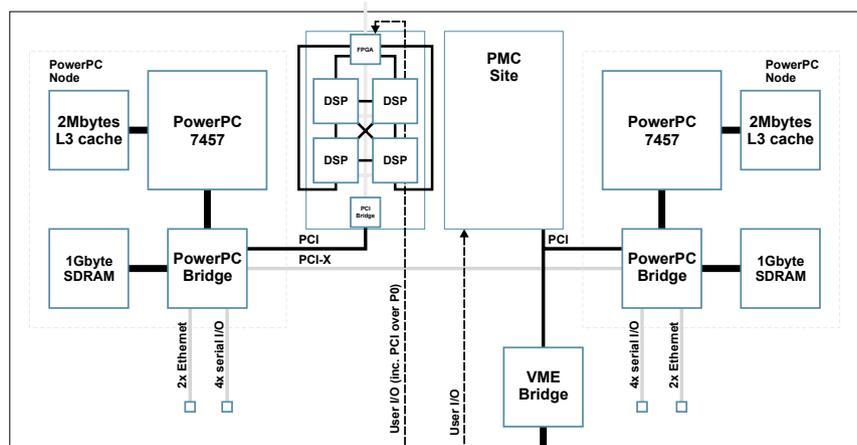
TS-C43

- 4x ADSP-TS101 DSPs.
- Local FPGA for direct external data I/O coupling to the DSP array including FPDP, LVDS and custom I/O modules.
- PMC format.

TS-V39

- 8x ADSP-TS101 DSPs.
- Local FPGAs for direct external data I/O coupling to the DSP array including FPDP, LVDS and custom I/O modules.
- VME format.

TigerSHARC DSP Modules



TVG5 fitted with DSP sub-system

FFT

- Fixed or block floating-point FFT/IFFTs.
- 32 to 8K points (call for Transtech for larger sizes).
- Window functions.

Digital Radar Receiver

- Decimation from 1 to 64
- Up to 511 channels
- Up to 511 taps per MAC engine
- Optional digital down conversion

QR Decomposition Processor

- Decomposition via Givens rotations
- Real or complex data
- User defined array size, dataset size and wordlength

Programmable Multi-Channel FIR Filter

- Up to 511 taps
- Decimation up to 64
- Up to 511 channels
- Real or complex data

Floating-Point Mathematics

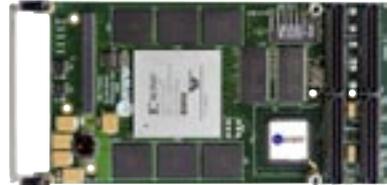
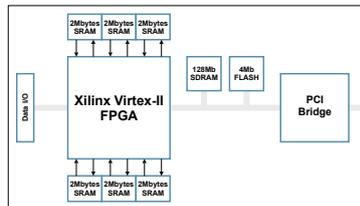
- Adder, multiplier, divider and square root
- Variable wordlength floating-point including IEEE-754 single & double precision wordlengths
- Fully parametrized

FPGA IP Cores

FPGA Co-Processor

Some applications have a performance requirement that only devices such as FPGAs and ASICs can achieve - the speeds of modern FPGAs mean that FPGAs are usually the most practical. This is because an FPGA is a truly parallel device that can absorb a number of functions such as large FFTs, Viterbi decoders and QR decomposition. Since FPGAs are re-configurable, they are extremely flexible and able to adapt to any number of applications using common hardware.

Transtech provides a number of FPGA solutions. These include Xilinx Virtex-II and Virtex-II Pro based PMC modules with direct data ports so as not to introduce data bottlenecks to feed the fast data processing engines of the FPGA. Working along side a PowerPC processor array, the FPGA module can be used to offload computational intensive, but relatively simple, processing tasks while the PowerPC CPUs can implement algorithms that are more sophisticated as well as handling the man-machine interfaces including graphics and networking. The FPGA modules use some of the latest generation high-capacity FPGAs, but to increase their resources, Transtech has added multiple pools of memory for storing large datasets such as image frames, lookup tables and intermediate calculations.



PMC-FPGA02 FPGA Module Overview

PMC-FPGA02 FPGA Module

PMC-FPGA01

- Xilinx Virtex-E FPGA (XCV300)
- 128Mbytes SDRAM
- 64-bit data I/O ports (routed to the front panel and PMC user IO)

PMC-FPGA02

- Xilinx Virtex-II FPGA (XC2V3000-8000)
- 6x 2Mbyte banks of QDR SRAM
- 128Mbytes SDRAM
- 2x 64-bit data I/O ports

PMC-FPGA03

- Xilinx Virtex-II Pro FPGA (XCVP50)
- 3x 2Mbyte banks of QDR SRAM
- 2x 28Mbytes SDRAM
- 8x RocketIO (Gbps serial IO)

FPGA Modules

To aid application development using the FPGA modules, Transtech provides a range of IP cores including FFTs, digital radar receivers, QR decomposition, FIR filter and floating-point arithmetic. These cores can be provided as is or as standalone functions without the need for VHDL code development - in effect, the FPGA module can be made to look like say a 'black box' FFT co-processor. This is achieved through a bespoke service to match the customer's requirements on functionality and performance. With or without the IP cores, the FPGA modules have been developed to allow complete freedom in what goes into the FPGA and what it is used for.

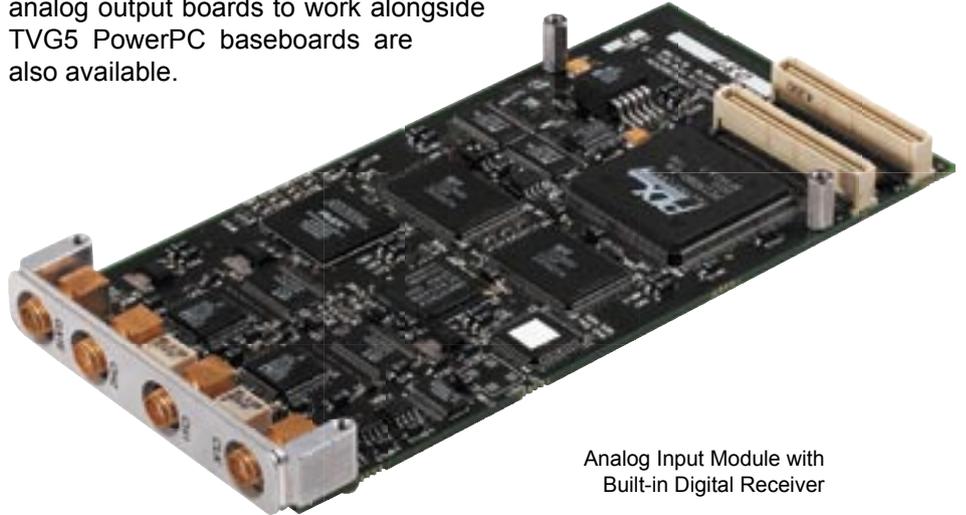
Data Input/Output

Digital Receivers/Modulators

Digital receivers/modulators with integrated analog I/O can be provided for applications ranging from software radio/surveillance to radar/sonar. Precision clock sources are also available.

Analog Input/Output

If digital receivers are not required with the analog I/O functions, then these features can be bypassed. Alternatively a range of pure analog input or analog output boards to work alongside TVG5 PowerPC baseboards are also available.



Analog Input Module with Built-in Digital Receiver

Digital Receivers/Modulators

- Narrow, wide and ultra wideband receivers and modulators
- Integrated analog inputs and outputs
- IFs to 250MHz (sampling up to 125MSPS)

Analog Input/Output

- Sampling from <100kHz to 1.5GHz
- Resolutions for 8 to 24-bit
- High channel densities per slot available

Digital Input/Output

- LVDS
- FPDP
- RS422
- Custom

Input/Output Modules

Digital Input/Output

High performance computing often requires high input/output data streams. The PMC-FPGA0x modules (see FPGA co-processors for details) are designed for this purpose with front panel adaptor modules including FPDP and LVDS for standard data equipment interfaces. The digital interfaces are controlled via local FPGAs which have the added benefit of being able to provide local data processor in real-time on the data stream. This might be something as simple as data packing for efficient data transfer to digital filters or lookup tables. If the necessary interfaces are not available, then the PMC-FPGA0x modules can still be used since new ones are easily developed either by Transtech DSP or in-house.



Adaptor modules for a range of DSP, FPGA and I/O boards, simplifies custom interfaces

System Input/Output

Graphics

Graphics Modules

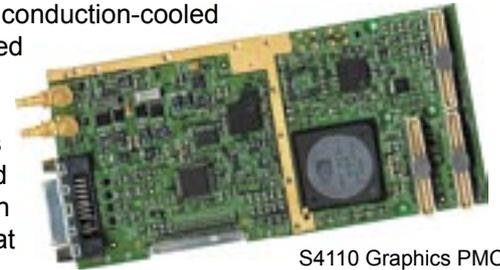
- Video Input: NTSC, PAL, RS-170, RS-170A and S-Video
- Video Output: DVI 1.0 analog and digital; LVDS (flat panel) digital single or dual link; composite or S-Video
- Resolution up to 2048x1536 (analog) or 1600x1200 (digital)
- OpenGL 1.3 support under VxWorks and Linux

Networking Module

- MIL-STD-1553
- ARINC 429
- Fibre-channel

System I/O Modules

Available in either convection or conduction-cooled variants, the S4110 module is based on an NVIDIA Quadro4 graphics unit that provides high resolution, multi-channel 2D & 3D graphics and advanced video input and output. The S4110 supports both analog output as well as digital flat panel displays.



S4110 Graphics PMC

Networking

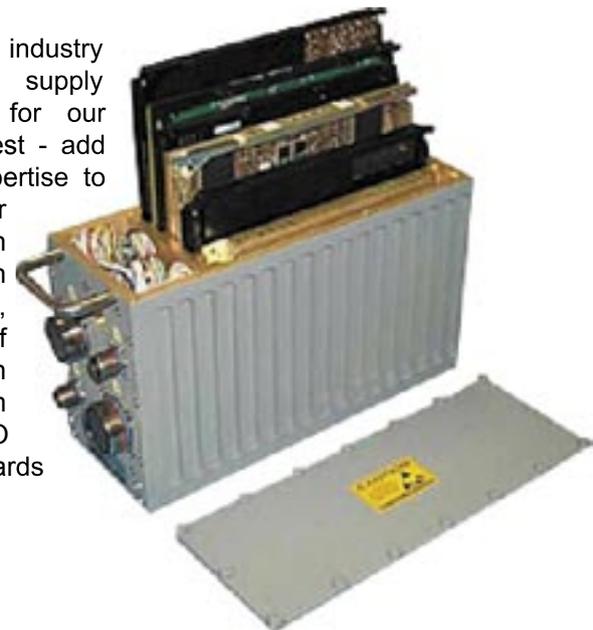
In addition to direct data I/O from either analog or parallel data sources and already included on the TVG5 processor card (fast Ethernet and serial I/O), there are a range of system I/O functions that can be supplied.

Systems Integration

The philosophy behind Pegasus is one of coherent simplicity: being able to source a collection of boards, modules and software, drawn from various industry specialists, and know they will work together with a single point of contact and support. Transtech, specialists in DSP based equipment (using PowerPC, FPGA and DSP technology), works with analog I/O, digital receivers, software, chassis suppliers to provide this single source of supply along with integration, custom design and consultancy service. This ranges from commercial/air-cooled solutions up to rugged/conduction-cooled.

A long history of experience with a wide variety of processor types (including PowerPC, C4x, C6x, SHARC, TigerSHARC, FPGA, Pentium) affords Transtech the know-how to mix and scale different processor elements effectively. For example, DSPs can be used for low power applications and FPGAs are ideal for intensive operations.

Through its experience and industry relationships, Transtech can supply a complete sub-system ready for our customers to do what they do best - add their intellectual property and expertise to deliver the complete system to their customer without needing to concern themselves with system integration issues. Other than boards, drivers, software tools and chassis, some of the integration tasks that Transtech can undertake include custom designs ranging from simple I/O transceivers & modifying existing cards up to complex board solutions.



Software

Pegasus systems are suitable for a wide range of applications, especially processor intensive and real-time. Several operating systems are available including VxWorks and Linux.

Along with Operating Systems, the Pegasus sub-systems roadmap includescan optimized DSP libraries such as VSIPL (an open standard suite for code portability), MPI (Message Passing Interface), run-time BIT (Built-In test) as well a wide variety of drivers, utilities and development tools.

VxWorks

VxWorks is an industry standard real-time operating system and is the run-time component of the Tornado II embedded development platform. Tornado II includes a comprehensive suite of cross-development tools & utilities and a full range of communications options from the host connection to the target. The microkernel supports a full range of real-time features, including fast multitasking, interrupt support, and both preemptive and roundrobin scheduling. The microkernel is designed to minimize system overhead and so enable fast, deterministic response to external events. The developer has many features available in the design of applications including using shared memory (for simple sharing of data), message queues, semaphores, events and pipes (for intertask messaging within a CPU), sockets and remote procedure calls (for network-transparent communication), and signals (for exception handling).

VSIPL - PowerPC DSP Library

Based on the DARPA definitions, the VSIPL library provides a core set of common DSP functions that are optimized for the PowerPC 74xx (AltiVec) CPUs. The basis behind the DARPA definition is to provide a processor and operating-system independent set of DSP functions thereby allowing for maximum code portability.

VSIPL API

- Over 500 functions
- DARPA sponsored
- PowerPC G4 (AltiVec) optimizations

VSIPL features

- Portability
- Object-based description
- Opaque objects such as blocks, and views on the blocks (vectors, matrices, and tensors)
- Development and production modes
- Public and private data arrays enabling implementation optimizations
- Explicit memory/algorithm hints

Functionality

- Scalar Functions
- Vector and Matrix (scalar, unary, binary, logical arithmetic, selection and data generation)
- Linear Algebra
- Signal Processing (FFTs, window, filter and convolution routines)
- Image Processing



www.transtech-dsp.com



20 Thornwood Drive, Ithaca, NY 14850-1263, USA
Tel: 607 257 8678 Fax: 607 257 8679
email: sales@transtech-dsp.com

Manor Courtyard, Hughenden Avenue, High Wycombe, HP13 5RE, UK
Tel: +44(0)1494 464432 Fax: +44(0)1494 464472
email: sales@transtech-dsp.com

11 Saharov Street NIA, Rishon LeZion 75707, Israel
Tel: 972-3-9518718 Fax: +972-3-9518719
sales@transtech-dsp.com

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