PMC/XMC Modules (EK-LVM)

EK-LVM
User-Programmable Xilinx Virtex-5 FPGA PMC/XMC Modules

Applications

- Remote Sensor Interface
- Radar & Sonar Systems
- In-flight & Shipboard Systems
- Electronic warfare, SIGINT, ELINT and Surveillance
- Real-time imaging, Inspection and Machine vision
- Data Recorders
- Distributed Processing Interconnect
- Protocol Converter
- Data Encryption
- Beam-forming
- DSP Processing

Features

- FPGA(Default) : XC5VLX85T-1FFG1136I (Industrial Temperature Range : -40 ~ 100℃)
- Temperature Range
  - Operating Temperature : - 40 ~ 85℃
  - Storage Temperature : - 50 ~ 105℃
- Programmable/Reconfigurable Xilinx Virtex-5 FPGA via JTAG-port with Flash Memory
- PCI(X) x 64bits BUS up to 133Mhz via PMC Connector (P11,P12,P13)
- PCI-Express up to 4 Lane (GEN1) via XMC Connector (P15)
- 4 Banks of 128MB x16 DDR2-SDRAM (Totally, 512MB)
- 64 User I/O's up to 32 pairs LVDS Interface via PMC Connector (P14)
- Front End plug-in I/O Connector (Future released)
- Power Source : 3.3V & 5.0V
- Signal Source : 5.0V Tolerant.
- Supports Xilinx ChipScope Pro Tool

Description

▪XC5VLX85T-FF1136 : 12,960 CLB(Configurable logic blocks) and 48 DSP48E Slices

▪EK-LVM cards support a reconfigurable Xilinx Virtex-5 FPGA enhanced with totally 512MB high-speed DDR2 Memory buffers and a high-throughput PCI-X(PMC) or PCI-Express x 4lane(XMC) Interface

▪EK-LVM cards are provided with up to 133MHz * 64bits PCI-X(PCI) Bus via the traditional PMC(P11,P12,P13) Connectors. And EK-LVM cards are provided with up to PCI-Express 4 lane (GEN1) interface via XMC(P15) connector. PCI-Express RX and TX lines are the point-to-point interface. So, PCI-Express is good for the simultaneous RX and TX communication application.

▪High speed DDR2-Memories are provided with 4 x 128MB DDR2-SDRAM, totally 512MB. On a count of the large buffering capacity, the high speed DMA transferring are available

▪266MHz DDR2 clock(533MHz) rate are supported on the current XC5VLX85T-1FFG1136

▪64 I/O lines are provided via the rear connector.

▪Additional I/O lines are provided via the front plug-in I/O connector (Future released)

▪Optional Front Mezzanine plug-in I/O modules (Future released)

Specifications

Section		Descriptions
Standards	PMC	❖ IEEE1386-2001 (CMC) ❖ IEEE1386.1-2001 (PMC) ❖ ANSI/VITA 39-2003 (PCI-X Auxiliary Standard for PMCs and...) ❖ PCI Local Bus Specification r3.0 ❖ PCIX Addendum to the PCI Local Bus Specification r1.0b / r2.0a ❖ INTA# interrupt supported
	XMC	❖ ANSI/VITA 42.0-2008 (XMC Basic Specification) ❖ ANSI/VITA 42.3-2006 (XMC PCI-Express) ❖ PCI-Express Release 1.1
Memory		❖ 4 banks of 128MB DDR2-SDRAM for buffering (Totally, 512MB)
I/O Interface	PMC	❖ P11~ P13 : PCI-X 66, 100, 133Mhz Interface ❖ P14 : Up to 32 pairs LVDS User 64 I/O's Interface
	XMC	❖ P15 : PCI-Express x 4 with 4 DMA channels up to 8Gbps
Environmental		❖ Operating Temperature : -40 ~ 85℃ ❖ Storage Temperature : -55 ~ 105℃ ❖ FPGA Temperature : -40 ~ 100℃
Design Kit		❖ Example FPGA source codes are provided with a DDR2-SDRAM Controller, LVDS Interface Sample Code,
Optional		❖ 4 DMA channel supported FPGA IP at a separate account. If you need it, you should order it with the purchase of this card.

Phone : 82-31-889-3216, Fax : 82-31-889-3218, Email : dongkue.ho@eonic.co.kr, Website : www.eonic.co.kr

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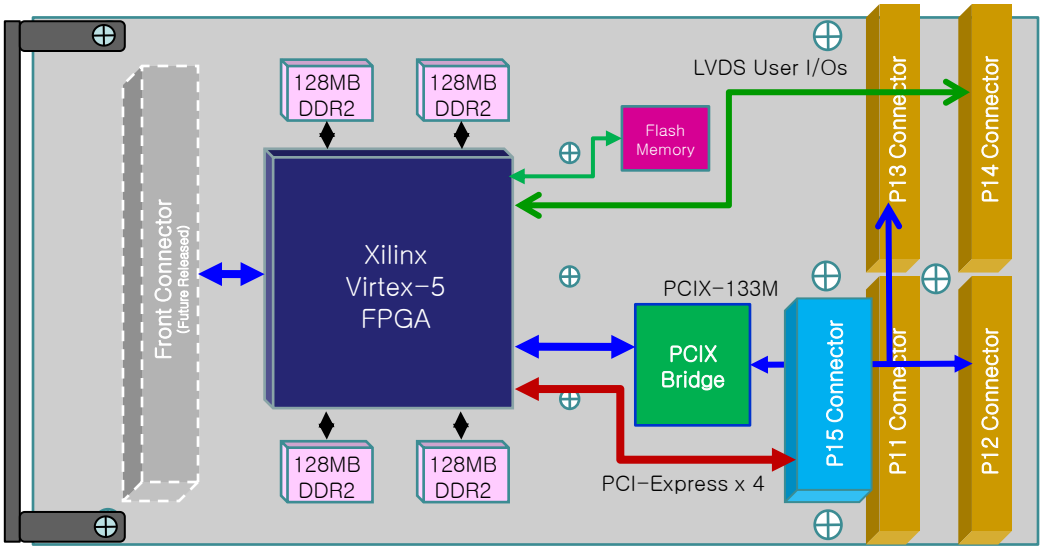
Block Diagram



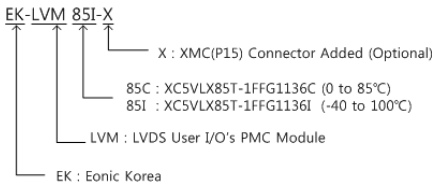
PMC P14 - I/O Pin Definition

Pin	Signal	Signal	Pin
1	USER_LVDS_N_0	USER_LVDS_N_1	2
3	USER_LVDS_P_0	USER_LVDS_P_1	4
5	USER_LVDS_N_2	USER_LVDS_N_3	6
7	USER_LVDS_P_2	USER_LVDS_P_3	8
9	USER_LVDS_N_4	USER_LVDS_N_5	10
11	USER_LVDS_P_4	USER_LVDS_P_5	12
13	USER_LVDS_N_6	USER_LVDS_N_7	14
15	USER_LVDS_P_6	USER_LVDS_P_7	16
17	USER_LVDS_N_8	USER_LVDS_N_9	18
19	USER_LVDS_P_8	USER_LVDS_P_9	20
21	USER_LVDS_N_10	USER_LVDS_N_11	22
23	USER_LVDS_P_10	USER_LVDS_P_11	24
25	USER_LVDS_N_12	USER_LVDS_N_13	26
27	USER_LVDS_P_12	USER_LVDS_P_13	28
29	USER_LVDS_N_14	USER_LVDS_N_15	30
31	USER_LVDS_P_14	USER_LVDS_P_15	32
33	USER_LVDS_N_16	USER_LVDS_N_17	34
35	USER_LVDS_P_16	USER_LVDS_P_17	36
37	USER_LVDS_N_18	USER_LVDS_N_19	38
39	USER_LVDS_P_18	USER_LVDS_P_19	40
41	USER_LVDS_N_20	USER_LVDS_N_21	42
43	USER_LVDS_P_20	USER_LVDS_P_21	44
45	USER_LVDS_N_22	USER_LVDS_N_23	46
47	USER_LVDS_P_22	USER_LVDS_P_23	48
49	USER_LVDS_N_24	USER_LVDS_N_25	50
51	USER_LVDS_P_24	USER_LVDS_P_25	52
53	USER_LVDS_N_26	USER_LVDS_N_27	54
55	USER_LVDS_P_26	USER_LVDS_P_27	56
57	USER_LVDS_N_28	USER_LVDS_N_29	58
59	USER_LVDS_P_28	USER_LVDS_P_29	60
61	USER_LVDS_N_30	USER_LVDS_N_31	62
63	USER_LVDS_P_30	USER_LVDS_P_31	64

Note1) The red letters I/O's can be also used as the clock source.

Ordering Information

❖ EK- Series Modules



❖ EK-LVM85-EDK
- Release to you, if EK-LVM PMC Modules are ordered

❖ Up to 4 x DMA Channel supported FPGA IP with Wrapper.
- Release to you, if you order it at additional cost.

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